Journal of Advanced Engineering Trends
ISSN : 2682 - 2091

Vol.43, No.1. January 2024

http://jaet.journals.ekb.eg

Improved Model of a Gallium Nitride HEMT for High Power Application

Gamal M. Dousoky [1,*], Fatma Ali [1], Mahmoud Abdelghany [1], Mohamed Abouelatta [2], Masahito Shoyama[3]

[1]*Department of Electrical Engineering, Faculty of Engineering, Minia University, Egypt*

[2]*Department of Electronics and Communications Engineering, Faculty of Engineering, Ain Shams University, Egypt*

[3]*Department of Electrical Engineering, Faculty of Information Science and Electrical Engineering, Kyushu University, Japan*

[*] *Corresponding Author E-mail: dousoky@mu.edu.eg*

A R T I C L E I N F O

Article history:
Received:
Accepted:
Online:

Keywords:
GaN
modeling
Capacitance

A B S T R A C T

In this paper, a development of Gallium Nitride -High-Electron-Mobility Transistor (HEMT) model is presented. Static characteristics are extracted from a commercial device data sheet and fitted into empirical functions using MATLAB software package. The stability performance of GaN devices is important to work in most of applications. The equivalent circuit model is tested in a simple configuration for plotting I-V curve through estimating parameters of the gate to drain capacitance (C_{GD}) and drain to source capacitance (C_{DS}). These parasitic capacitances are essential to provide a comprehensive understanding of the switching behavior of the device as well as critical parameters to enhance model static current-voltage characteristics .A stable performance of *I-V* curve has been achieved when using the proposed improved model equations of those capacitances. The obtained results show that the proposed model of Gallium Nitride -HEMT is favorable for use in high frequency, high efficiency, and high power density power conversion applications.

1. Introduction

GaN (Gallium Nitride) is one of the most interesting semiconductor materials owing to its unique electrical properties, which include a wider bandgap, thermal conductivity, and higher critical breakdown electric field. It is used in a variety of applications, including high efficiency, high frequency, and high power density power conversion applications [1]–[3]. The GaN HEMT is presently available from a number of companies, such as EPC (Efficient Power Conversion) Corporation, GaN Systems, International Rectifier (formerly developed by Infineon), Transphorm. GaN HEMTs have larger advantages than Si MOSFETs because they have a smaller RON (on-state resistance), high electric field, and a low parasitic capacitance [4]. GaN HEMTs can switch at higher rates because they have smaller switching and conduction losses [5]–[8]. Power electronics designer's demand circuit-oriented device models have been validated to analyse GaN HEMT performance in diverse applications, since the performance of power semiconductor devices is essential in power electronics applications. GaN transistor structures and circuit designs have been extensively investigated for power electronics applications [9]–[11].

Characterization and modeling of GaN transistor devices are also essential for high-power applications.The goal of this research is to improve a simple commercial available GaN HEMT devices and to test it under static conditions. So far, various GaN HEMT device models have been presented, most of which are based on the physics of the device. These device models established in physics are more exact, but they have a few drawbacks: they are complex, and they take a lot of time to simulate [4]. To use the model on a certain device, they usually require an enormous number of parameters of the device (which are frequently out of reach for designers of circuits). Furthermore, most of these kinds were developed for microwave or RF applications, which are little outside of the switching frequency band of power electronics.

In the power conversion literature, only a few studies on the modeling of devices for GaN HEMTs have been published [12]-[13]. [14]-[15] explain the design and validation of a basic device model for the Gallium Nitride HEMT in the current conduction in both reverse and forward channels. Additionally, this model is unique in that it is usable in the third quadrant, which is critical when the device is used as a freewheeling diode. EPC 2001 (100V/25A is the device under study, which is available for purchase. Figure 1 presents the GaN HEMT model's common structure. However, the parameter equations for the parasitic capacitances of this model do not provide stability performance of I-V curve for all commercial devices of GaN HEMT.

The equivalent circuit for a model of GaN HEMT is verified in a simple structure for the simulation I-V curve of variable parameters. In [16, 17], the Panasonic GIT (Gate Injection Transistor) [18] is the commercial device modeled in that paper, and its data sheet is open to the public. The recessed HEMT operates by reducing the thickness of the AlGaN barrier in the channel, resulting in a two-dimensional electron gas (2DEG). On the other hand, the Panasonic GIT turns off at zero gate bias, because it has a p-doped layer of the GaN below the gate electrode that helps to increase the conduction band much above Fermi level [19].

Revised:14 June , 2022, Accepted:10 August , 2022

This research focuses on enhancing the performance of the GaN HEMT model parameters (capacitance CGD, CDS) by extracting data sheets; which is then fitted using MATLAB software package. Then implementing these fitted equations of capacitance in the whole model of the transistor. For validating this model using MATLAB Simulink, the I-V curve has been plotted using the fitted equations; which provided a better behavior in the linear region, and on the contrary, the behavior is not acceptable when using fixed parameters. The commercial device used in this research is the GS61008P GaN systems [20].

This manuscript is ordered as follows: Section 2 presents the device simulation model. Then, the parasitic capacitance extraction and fitting are explained in Section 3. after that, Section 4. discusses the performance enhancement of the GaN-HEMT device. Finally, conclusions are summarized in Section 5.

2. Model for device simulation

Fig. 1 illustrates the circuit GaN HEMT model [21] obtained in this research for simple circuit simulation. I_{DS}, a voltage dependent current source, three parasitic resistances R_G R_D, and RS, two capacitance C_{DS} and C_{GD} which are voltage-dependent, and a gate-source capacitance CGS which is voltage independent, are all included in the model. With forward and reverse conduction, the I_{DS} source is employed to describe characteristics of static current-voltage *(I-V)*. The three parasitic capacitances are important in affecting the performance of the switching for the device. The parasitic capacitances and resistances are required to understand the device's performance in the switching. The current I_{DS} source is a bidirectional that is used in reverse conduction simulation for GaN HEMT.

2.1. Current Source Voltage-Dependent (I_{DS})

The I_{DS} is a function of internal device node voltages V_{gs} and V_{ds}. A positive V_{gd}, as well as a positive V_{gs}, will improve channel conduction because the device's lateral structure is almost symmetrical. As a result, both reverse and forward channel conduction modes are considered. The circuit model uses an exact temperature dependent device constant Kp to properly forecast the performance of the power converter at various temperatures.

There are four different operating modes: reverse saturation, reverse linear, forward saturation, and forward linear regions. Table 1 shows current equations of operating regions, where Vth1, Vth2 are threshold voltages for forward and reverse channel conduction, respectively. It's important to note the effect of the temperature on this model is ignored at threshold voltages. Kp1, Kp2 are transconductance parameters for temperature dependent device in forward and reverse conduction mode, respectively.

λ_1 is the channel length modulation parameter for forward channel conduction.

2.2. Parasitic Capacitances

This model uses constant C_{GS}, since C_{GS} is unaffected by the voltage applied to the electrodes. The capacitance of the device measurement shown in Figure 2 supports this assumption. The parasitic capacitances C_{GD} and C_{DS} are nonlinear voltage dependent and given by:

$$C_{GD}=\frac{C_{GD0}}{(1+\frac{|V_{gd}|}{PB1})^{m_1}} \quad (1)$$

$$C_{DS}=\frac{C_{DS0}}{(1+\frac{|V_{ds}|}{PB2})^{m_2}} \quad (2)$$

The Gate to Drain capacitance at zero-bias is C_{GD0}, while the Drain to Source capacitance at zero bias is C_{DS0}. The junction built-in potential PB1 for C_{GD} (Gate-Drain capacitance) and PB2 for C_{DS} (Drain-Source capacitance). The coefficient of junction grading is the parameter m1 for C_{GD}, while junction grading coefficient is the parameter m2 for Drain–Source capacitance C_{DS}.

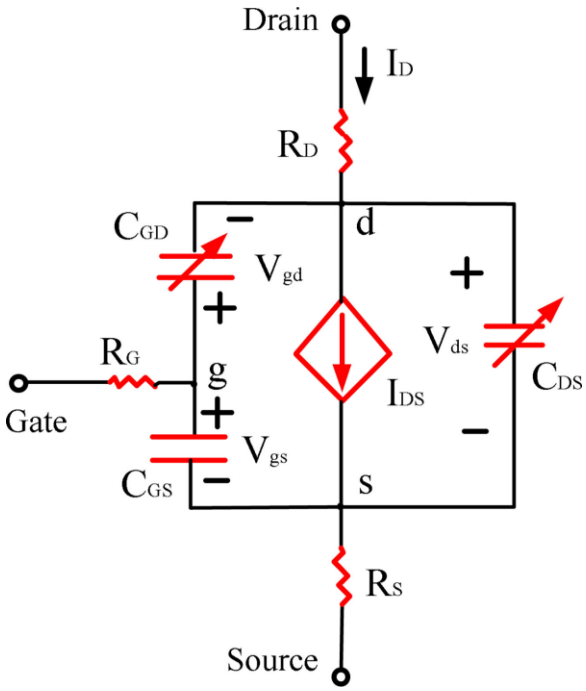


Figure 1: Circuit model of the GaN HEMT [21].

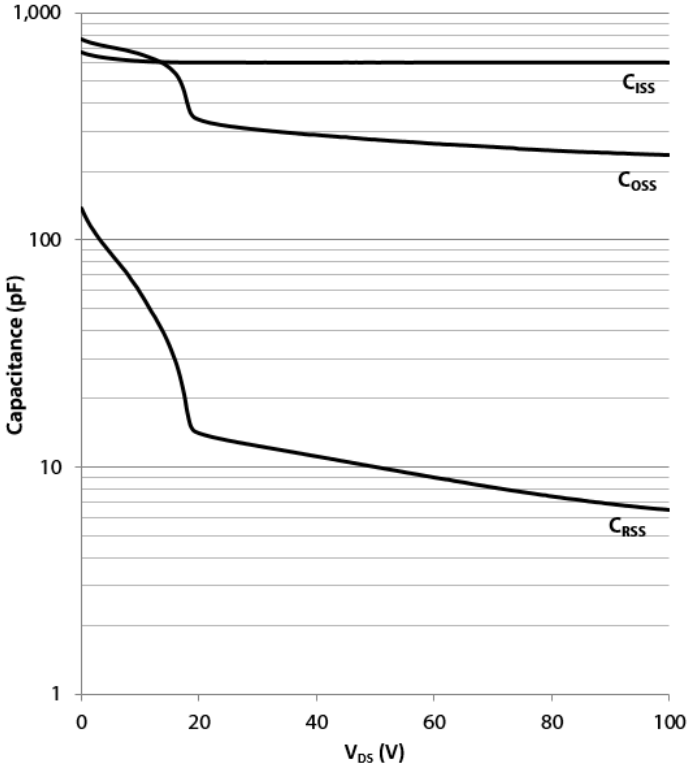


Figure 2: Capacitances measured versus V_{DS} for GS61008P [20].

Table 1: Voltage-dependent current source operating regions [14, 15]

Operating region	Condition	Equation
Cut off	$V_{gs} < V_{th1}$, $V_{ds} \geqslant 0$ or $V_{gd} < V_{th2}$, $V_{sd} \geqslant 0$	$I_{ds} = 0$
Forward conduction linear Region	$V_{ds} < V_{gs} - V_{th1}$ and $V_{ds} > 0$	$I_{ds} = K_{p1}\,[(V_{gs} - V_{th1})\,V_{ds} - V_{ds2}/2]$
Forward conduction saturation region	$V_{ds} > V_{gs} - V_{th1} > 0$ and $V_{ds} > 0$	$I_{ds} = K_{p1}\,(V_{gs} - V_{th1})^2\,(1 + \lambda_1 V_{ds})/2$
Reverse conduction linear Region	$V_{sd} < V_{gd} - V_{th2}$ and $V_{sd} > 0$	$I_{ds} = -K_{p2}[(V_{gd} - V_{th2})V_{sd} - V_{sd2}/2]$
Reverse conduction saturation region	$V_{sd} > V_{gd} - V_{th2} > 0$ and $V_{sd} > 0$	$I_{ds} = -K_{p2}\,(V_{gd} - V_{th2})^2/2$

The parasitic capacitance was extracted from the data sheet as a voltage dependent drain to source nonlinear capacitance. In power electronics applications, C_{rss} , C_{iss}, and C_{oss} capacitances are significant parameters measurements which are involved on the data sheet [20]. Equations (3)-(5) were required to translate the parameters into useful C_{GD}, C_{GS}, and C_{DS} in an effort to allow this essential information for the equivalent model.

$$C_{oss} = C_{GD} + C_{DS} \quad (3)$$

$$C_{iss} = C_{GS} + C_{GD} \quad (4)$$

$$C_{rss} = C_{GD} \quad (5)$$

2.3. Parasitic Resistances

When compared to the external resistance of the gate generally used to damp transient oscillations during switching transients, the internal resistance in the gate Rg is supposed to be the value of zero. Rs and Rd are the constant resistances which denote the distributed nature of the terminal contact mesh.

2.4. Transconductance Parameter K_p

The device model should incorporate a transconductance parameter which is the temperature dependency on the device, in order to correctly predict the loss in device conduction versus temperature. The voltage drop across the device as a function of current is determined by Kp:

$$K_p = K_{p0}/(1 + T_{C1}(T - T_0) + T_{C2}(T - T_0)^2) \quad (6)$$

The nominal parameter transconductance for a device at room temperature is K_{p0}, the nominal room temperature is T_0, and the temperature coefficients are T_{C1} and T_{C2}. Table 2 contains the required parameters for the GaN HEMT model under consideration.

Table 2: parameters of GaN HEMT model [14, 15]

V_{th1}	**Threshold voltage for forward conduction gate**
V_{th2}	**Threshold voltage for reverse conduction gate**
K_{p1}	**Transconductance parameter for forward conduction device at room temperature**
K_{p2}	**Transconductance parameter for reverse conduction device at room temperature**
λ_1	**Channel length modulation coefficient for forward conduction**
C_{GS}	**Gate to Source capacitance**
C_{GD0}	**Gate to drain capacitance with zero bias**
PB1	**Built-in potential for gate to drain capacitance**
m_1	**Junction grading coefficient for gate to drain capacitance**
m_2	**Junction grading coefficient for drain to source capacitance**
PB2	**Built-in potential for drain to source capacitance**
C_{DS0}	**Drain to source capacitance with zero bias**
R_d	**Parasitic resistance for the drain**
R_s	**Parasitic resistance for the source**
T_{C1-1} T_{C2-1}	**Temperature coefficients for forward conduction device constant**
T_{C1-2} T_{C2-2}	**Temperature coefficients for reverse conduction device constant**

3. Parasitic capacitances extraction and fitting

The C-V curves have been found and exponential formulas were used to fit them. The better matched is obtained in the C-V curves and is shown in Figures 3, 4, and 5 for C_{oss}, C_{iss}, and C_{rss}, respectively. When terminals of the source and gate are shorted, C_{oss} represents small signal output capacitance. When the source and drain terminals are both shorted, C_{iss} is the small signal input capacitance, and C_{rss} is the small signal reverse transfer capacitance. To curve fitting is accomplished using MATLAB.

Many functions have been tested, and the exponential one proved its superiority due to its nature; which matches the fitted curves. The fitted equations (1)-(3) [16], [17], for C_{DS}, C_{GS}, C_{GD}, and are acquired and are shown in equations (7)-(9), in pF (Pico Farads):

$$Crss = 908.32e^{(-0.03.5443V_{ds})} + 12474e^{(-481.16V_{ds})} + 11703e^{(-0.049613V_{ds})} \quad (7)$$

$$C_{iss} = 65.006e^{(-0.23172V_{ds})} + 612.38e^{(-0.0001336V_{ds})} \quad (8)$$

$$C_{oss} = 227.57e^{(0.00058588V_{ds})} + 591.03e^{(-0.051982V_{ds})} \quad (9)$$

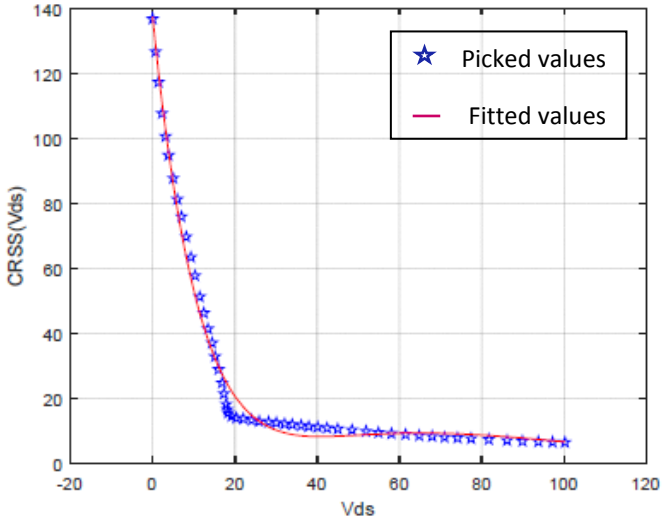


Figure 3: Reverse capacitance (C_{rss}) extraction and fitting.

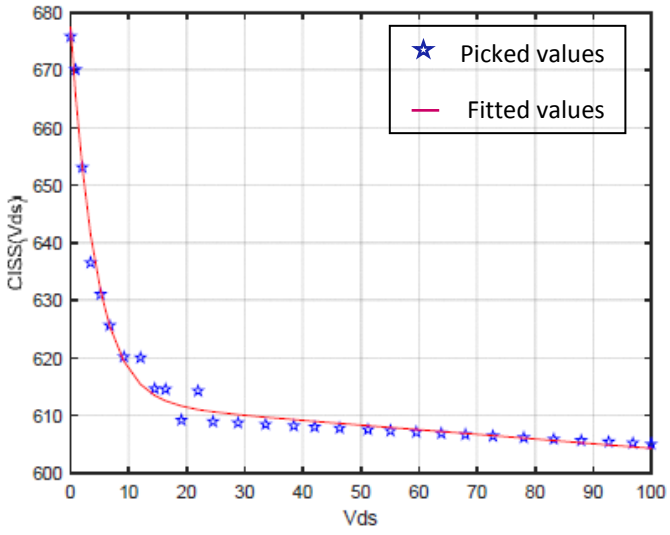


Figure 4: Input capacitance (C_{iss}) extraction and fitting.

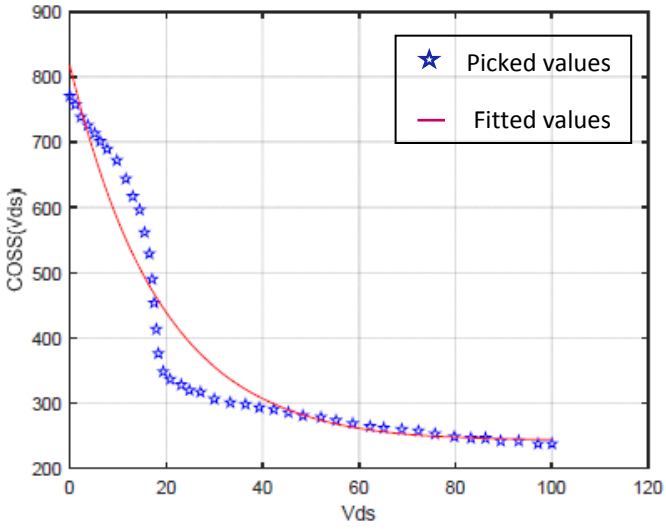


Figure 5: Output capacitance (C_{oss}) extraction and fitting.

4. Enhanced Performance of the GaN-HEMT device

Figure 6 displays the typical I-V curves for GS61008P GaN-HEMT at standard room temperature (25^0 C). A sample of comparison between drain-source current (I_{DS}) using the model performance in Simulink of the GaN-HEMT switching device at V_{gs}=6V and V_{ds}=4.5V in figure 7. As shown in figure 7(a), oscillation in the saturation region of the I-V curve is attained when using capacitance obtained from Equations (1)-(5). However, performance is improved (becames stable) when using the parasitic capacitances obtained by extraction and fitting, addressed in Equations (7)-(9), as shown in Figure 7(b), which promotes high power applications. The obtained results of the simulation have a close matching with experimental results for figure 6 at Vgs= 6V at standard room temperature (25^0 C). Extracted model parameter values for GS61008P are addressed in Table 3.

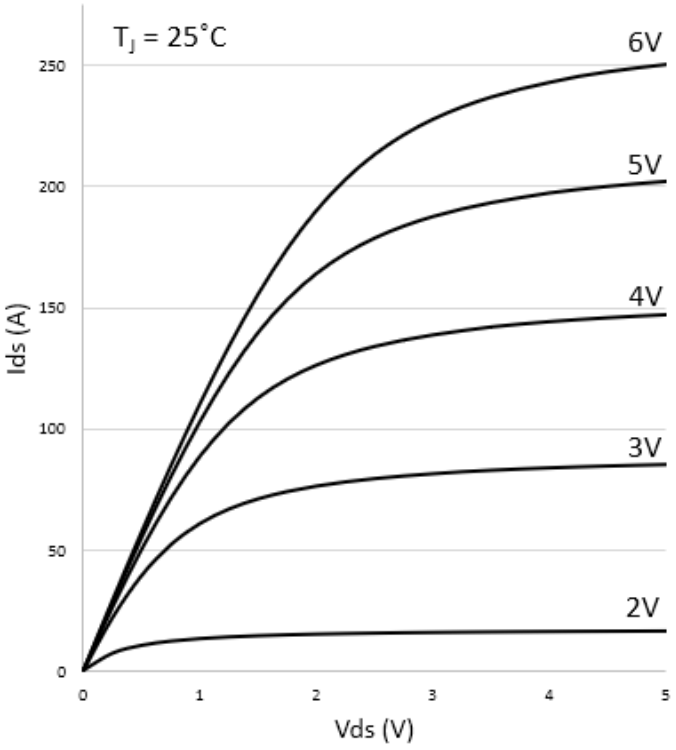
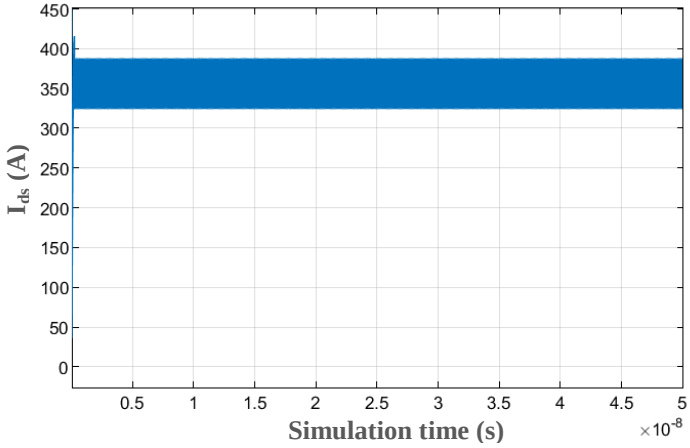
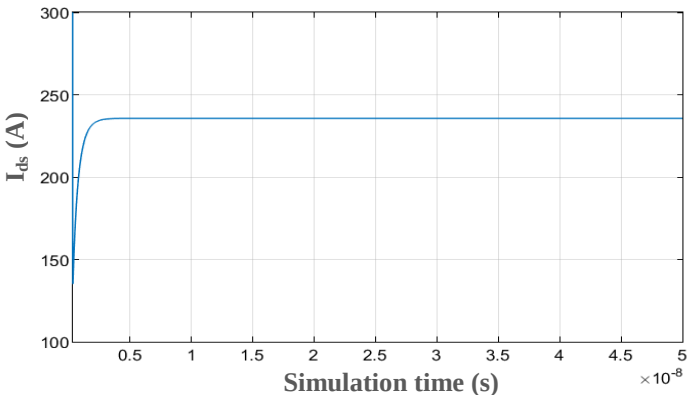


Figure : 6 Typical I_{DS} vs. V_{DS} characteristic at $T_J = 25^0$ C for GS61008P GaN-HEMT [20].



(a) Unstable performance attained when using capacitance obtained from Equations (1)-(5).



(b) Stable performance attained when using capacitance obtained by extraction and fitting

Figure 7: A sample of comparison between I_{ds} using the model performance of the GaN-HEMT switching device at V_{gs}=6V and V_{ds}=4.5V.

At the above-mentioned operating point (V_{ds} = 4.5V and V_{gs} = 6V), the Ids should have a stable value of around 240A (from Fig. 6). This has been achieved in Fig. 7(b) using the improved model. However, an unstable operation has been obtained (shown in Fig. 7(b)) using the conventional model.

5. Conclusions

In this paper, an improved model of GaN HEMT device is developed for circuit simulators. The parasitic capacitance curves were extracted from a datasheet of the commercial device (GS61008P GaN-HEMT) and best fitted using MATLAB software package with exponential expressions. These obtained parasitic capacitance functions are closely matched with C_{oss}, C_{iss}, and C_{rss} addressed in data sheet. These parasitic capacitances are essential to enhance the performance of the switching device. After using the proposed improved model functions of those capacitances in the model of GaN-HEMT using Simulink, a stable performance is achieved without oscillations. As a result, the proposed model of GaN-HEMT is a promising solution for high temperature and high power density power conversion applications.

Table 3: Parameter values extracted for GS61008P

Parameter	Value	Source
K_{p1-25}	19.6371 A/V^2	Characteristics of DC transfer curves
K_{p2-0}	6.2715 A/V^2	Characteristics of DC transfer curves
V_{th1-25}	0.3627 V	Characteristics of DC transfer curves
V_{th2}	-1.4303V	Characteristics of DC transfer curves
λ_1	9.1A/V	DC output characteristics
C_{GS}	577.6 pF from datasheet, (596 pF from curves)	Characteristics of the C-V curves
C_{GD0}	130pF	Characteristics of the C-V curves
PB1	1.2868 V	Characteristics of the C-V curves
m_1	0.899	Characteristics of the C-V curves

C_{DS0}	640pF	Characteristics of the C-V curves
PB2	1.6891 V	Characteristics of the C-V curves
m_2	0.1765	Characteristics of the C-V curves
R_d	7mΩ (from datasheet)	DC output characteristics
T_{C1}	0.0148	Temperature
T_{C2}	0.002 (assumed)	Temperature

References

[1] E. Santi, K. Peng, H. A. Mantooth, and J. L. Hudgins, "Modeling of wide-bandgap power semiconductor devices-part II, "IEEE Trans. Electron Devices, vol. 62, no. 2, pp. 434–442, Feb. 2105.

[2] U. K.Mishra, P. Parikh, and Y.Wu, "AlGaN/GaN HEMTs—An overview of device operation and applications," in Proc. IEEE vol. 90, no. 6, pp. 1022–1031, Jun. 2002.

[3] M. A. Khan, G. Simin, S. Pytel, A. Monti, E. Santi, and J. L. Hudgins, "New developments in gallium nitride and the impact on power electronics," in Proc. IEEE Power Electron. Spec. Conf., Jun. 2005, pp. 15–26.

[4] A. Lidow, J. Strydom, M. de Rooij, and Y. Ma, GaN Transistors for Efficient Power Conversion. El Segundo, CA, USA, Power Conversion Publications, 2012.

[5] R. Mitova, R. Ghosh, U. Mhaskar, D. Klikic, M. Wang, and A. Dentella, "Investigations of 600 V GaN HEMT and GaN diode for power converter applications," IEEE Trans. Power Electron., vol. 29, no. 5, pp. 2441–2452, May 2014.

[6] X. Huang, Z. Liu, Q. Li, and F. C. Lee, "Evaluation and application of 600 V GaN HEMT in cascode structure, "IEEE Trans. Power Electron., vol. 29, no. 5, pp. 2453–2461, May 2014.

[7] B. Wang, M. Riva, J. D. Bakos, and A. Monti, "Integrated circuit implementation for a GaN HFET driver circuit," IEEE Trans. Ind. Appl., vol. 46, no. 5, pp. 2056–2067, Sep./Oct. 2010.

[8] T. Ishibashi et al., "Experimental validation of normally-on GaN HEMT and its gate drive circuit," IEEE Trans. Ind. Appl., vol. 51, no. 3, pp. 2415–2422, May/Jun. 2015.

[9] R. Mitova, R. Ghosh, U. Mhaskar, D. Klikic, M.-X. Wang, and A. Dentella, "Investigations of 600-V GaN HEMT and GaN diode for power converter applications," IEEE Trans. Power Electron., vol. 29, no. 5, pp. 2441–2452, May 2014.

[10] X. Huang, Z. Liu, Q. Li, and F. C. Lee, "Evaluation and application of 600 V GaN HEMT in cascode structure," IEEE Trans. Power Electron.,vol. 29, no. 5, pp. 2453–2461, May 2014.

[11] D. Reusch and J. Strydom, "Understanding the effect of PCB layout on circuit performance in a high-frequency gallium-nitride-based point of load converter," IEEE Trans. Power Electron., vol. 29, no. 4, pp. 2008–2015, Apr. 2014.

[12] K. Shah and K. Shenai, "Simple and accurate circuit simulation model for gallium nitride power transistors," IEEE Trans. Electron Devices, vol. 59, no. 10, pp. 2735–2741, Oct. 2012.

[13] R. Khanna, W. Stanchina, and G. Reed, "Effects of parasitic capacitances on gallium nitride hetero-structure power transistors," in Proc. IEEE Energy Convers. Congr. Exhib., 2012, pp. 1489–1495.

[14] K. Peng and E. Santi, "Characterization and modeling of a gallium nitride power HEMT," 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, 2014, pp. 113-120, doi:10.1109/ECCE.2014.6953383.

[15] K. Peng, S. Eskandari and E. Santi, "Characterization and Modeling of a Gallium Nitride Power HEMT," in IEEE Transactions on Industry Applications, vol. 52, no. 6, pp. 4965-4975, Nov.-Dec. 2016, doi: 10.1109/TIA.2016.2587766.

[16] Garcia, Frances & Shamsir, Samira & Islam, Syed & Tolbert, Leon. (2018). A SPICE Model for GaN-Gate Injection Transistor (GIT) at Room Temperature. International Journal of High Speed Electronics and Systems. 27. 1840017. 10.1142/S0129156418400177.

[17] Garcia, Frances D., "A Physics-Based Analytical Compact Model, TCAD Simulation, and Empirical SPICE Models of GaN Devices for Power Applications." Master's Thesis, University of Tennessee, 2018. https://trace.tennessee.edu/utk_gradthes/5342

[18] Panasonic, GaN-Tr N-channel enhancement mode FET, PGA26E07BA datasheet, Sept. 2016 (Revised Jan. 2017).

[19] Z. Wang, B. Zhang, W. Chen, and Z. Li, "A closed-form charge control model for the threshold voltage of depletion and enhancement-mode AlGaN/GaN devices," IEEE Transactions on Electron Devices 60(5), 1607-1612 (2014).

[20] GS61008P Bottom-side cooled 100 V E-mode GaN transistor Preliminary Datasheet, available at https://gansystems.com/wpcontent/uploads/2018/04/GS61008P-DS-Rev-180420.pdf

[21] K. Peng, S. Eskandari, and E. Santi, "Characterization and Modeling of Gallium Nitride Power HEMT," IEEE Transactions on Industry Applications, 52(6), 4965-4975 (2016).