IMPROVED PERFORMANCE OF LNA USING HIGH QUALITY FACTOR PGS ON-CHIP SPIRAL INDUCTORS

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Abstract

This paper presents a detailed study of on-chip spiral inductors with patterned ground shield (PGS) inserted between the spiral inductor and the silicon substrate. This new design has been implemented in source degeneration cascode low noise amplifier (LNA) circuit to show how the PGS inductors improve the performance of the circuit. An operation in 1.8V supply voltage, source degeneration cascode LNA structure was studied with both technology and PGS inductors. In this paper, the Agilent ADS (Advanced Design System) simulation software and TSMC 0.18μm CMOS process parameters were adopted to achieve the low-cost characteristics and high integration to fit the performance of 2.4 GHz LNA design under IEEE 802.11a specification. According to the co-simulation results, the forward gain (S21) improved from 13.432 to 21.474 dB, and the (S12) is below the typical value of -15dB. The input impedance (S11) and the output impedance (S22) also represented good performance. In addition, the minimum noise figure was quite good. Thus, the LNA circuit with PGS inductors was better in the availability and the possibility of 802.11a specification.

Keywords: on-chip inductors, patterned ground shield, cascade amplifier, IEEE 802.11a.

1. Introduction

Inductors are one of the key factors that determine the performance of RF-IC’s. Among them, spiral inductors receive great attention due to their relatively high performance. It is frequently used in voltage-controlled oscillators (VCO’s), low noise amplifiers (LNA’s), mixers, and intermediate frequency filters (IFF’s). There are two types of on-chip inductors: bond-wound and planar spiral inductor. The planar spiral inductor has advantages of minimizing the chip size, reducing wiring requirement, and delay time. Currently, there are many types of planer spiral inductors according to its geometry: square, hexagonal, octagonal and circle.

The need for integrated circuits with high Q-factor’s inductors has been increasing recently. The spiral inductors on Si-based RFICs have suffered from low Q-factor due to their capacitive and electromagnetic coupling with the substrate at high frequencies. Therefore, it is one of the most intensively researched topic in RFICs. The Q-factor of the inductor is limited by the resistive losses in the spiral coil and by the substrate losses. Previous works have been done for improving the Q-factor of on–chip inductors, layout optimization, non-uniform metal width and non-uniform coil spacing, parallel current path, differential excitation, negative resistance, and a pattern ground shield (PGS) [1-6]. Because of the advantages of the PGS, we will use it to enhance the Q-factor of the three inductors.

The LNA is a key component that is typically placed at the front end of a radio receiver circuit. By using a low noise amplifier, the effect of noise from subsequent stages of the receiving chain is diminished by the gain of the amplifier. The radio frequency receivers consider (LNA) as their backbone. In this work, it has been used as a test circuit.
2. Modeling of spiral inductor

A lumped circuit model of on-chip spiral inductor grown on Si substrate is shown in Figure (1) [7]. \( L_s \) and \( r_s \) are the series inductance and resistance of the spiral respectively. \( C_s \) is the overlap capacitance between the turns of spiral and the cross-under layer. \( C_{ox} \) is the oxide capacitance between the spiral and the substrate. \( R_{si} \) and \( C_{si} \) are the parameters modeling substrate losses and capacitive effects, respectively.

![Fig. 1: Lumped model of a spiral inductor](image)

The inductance of a spiral is a complex function of its geometry and includes both self and mutual inductances. The expressions for on-chip spiral inductor parameters are given by [7]:

\[
L_s = \frac{\mu l}{2\pi} \left\{ \ln \frac{l}{2N(w+t)} + 0.5 + \frac{4N(w+t)}{3l} - 0.47N + (N-1) \right\}
\]

\[
r_s(\omega) = \frac{l}{\omega \sigma \delta(\omega)} \left( 1 - e^{-\frac{l}{\delta}} \right)
\]

\[
C_{ox} = l \cdot w \cdot \frac{\varepsilon_{ox}}{t_{ox}}
\]

\[
C_s = N \cdot C_{ov} = N \cdot w^2 \cdot \frac{\varepsilon_{ox}}{d}
\]

\[
R_{si} = \frac{2}{l \cdot w \cdot c_{sub}}
\]

\[
C_{si} = \frac{2}{l \cdot w \cdot c_{sub}}
\]

where \( l \) is the wire length, \( w \) is the width of the metal conductor, and \( t \) is the thickness of the metal conductor.

There are basically three types of capacitances in an on-chip inductor[8]:

1. the series capacitance \( C_s \) between metal lines, is given by:

\[
C_s = n \cdot w^2 \cdot \frac{\varepsilon_{ox}}{t_{ox,M1-M2}}
\]

where \( n \) is the number of overlaps, \( w \) is the spiral line width, and \( t_{ox,M1-M2} \) is the oxide thickness between the spiral.

2. the oxide capacitance \( C_{ox} \) associated with the oxide layer, is given by:

\[
C_{ox} = \frac{1}{2} \cdot l_t \cdot w \cdot \frac{\varepsilon_{ox}}{t_{ox}}
\]

where \( t_{ox} \) is the oxide thickness underneath the metal.
the coupling capacitance $C_{sl}$ associated with the Si substrate, is given by:

$$C_{sl} = \frac{1}{2} \cdot l_t \cdot w \cdot C_{sub}$$  \hspace{1cm} (9)

where $C_{sub}$ is the capacitance of the substrate.

3. LNA Circuit Structure

Figure 2(a) shows the complete schematic circuit of 2.4 GHz cascode LNA. The method employed here is inductive source degeneration. The degeneration inductor ($L_2$) enables more flexibility in matching the input stage to 50Ω. It is also used to improve the stability and linearity of the LNA. Inductive load ($L_3$) at the drain of cascading transistor compensates for the degradation in gain at high frequency. This inductor is used to set the resonant frequency. The greater the value of $L_3$, the greater will be the gain. Nevertheless, it is not practical to make $L_3$ very high, because high inductive values will result in low self-resonant frequency. Accordingly, the nominal value of 4.1nH is chosen for $L_3$ [9]. Cascoding transistor is used to reduce the interaction of the gate-drain capacitance of lower transistor and also improves the reverse isolation $S_{12}$. This topology is one of the most popular LNA topologies due to its merit of low power consumption, high gain, and high reverse isolation. In the design of low noise amplifiers, there are several common goals. These include noise figure ($NF$), Gain, linearity, input and output matching, power consumption, and stability. Figure 2(b) shows the same circuit, but with PGS inductors instead of the technology inductors, which will be discussed later.

In this section, three inductors have been designed using Momentum optimization tool of ADS2009, which exist in the previous LNA circuit (see Fig.1(a)). Momentum is a three-dimensional planar electromagnetic (EM) simulator that enables RF and microwave designers to significantly expand the range and accuracy of the passive circuits and circuit models [10]. Figure 3(a) shows the layout of the inductive load ($L_3$), which has 5.5 turns, a radius of 30 μm, and width of 6 μm on metal layer 6. Figure 3(b) shows the layout of the matching inductor ($L_4$), which has 5.5 turns, a radius of 40 μm, and width of 6 μm on layer 6. Figure 3(c) shows the layout of The source degeneration inductor ($L_2$), which has half turn, a radius of 40 μm, and width of 6 μm on layer 6.
There are other advantages of PGS such as; 1- the behavior of the inductor, which is easier to model, especially at different temperatures, 2- Inductor behavior is independent of variations in substrateresistivity and type (e.g. bulk, epi and SOI). [8]. Figure 3(d) shows the inductive inductor with PGS simulated with the momentum tool of ADS 2009. Note that the slots in the PGS are orthogonal to the direction of current flow in the spiral inductor to increase the resistance to the image current [11]. Similar behavior is shown in Fig.3(e) and 3(f) for the matching inductor with PGS and the source degeneration inductor with PGS, respectively.
4. Results and Discussion

4.1 Spiral inductor with and without shield:

The simulation results of the Q-factor with frequency for the conventional L2, L3 and L4 and PGS inductors are shown in Figures (4), (5), and (6) respectively. It can be noticed that at 2.4 GHz, the Q-factor of the PGS inductor was enhanced by approximately 65%. For the matching inductor, the Q-factor enhanced by 60%. Regarding the source degeneration inductor, it has a different shape because it has a half turn, even though, the enhancement percentage was 40.6%.

![Comparison of the Q-factor versus frequency of inductive inductor with and without PGS.](image)

Fig.3: (a) layout of the The inductive load (L3), (b) layout of the The matching inductor (L4), (c): layout of The source degeneration inductor (L2), (d): layout of the the inductive inductor with PGS, (e): layout of the matching inductor with PGS, (f): layout of The source degeneration inductor with PGS.
4.2 Co-simulation results:
S-Parameter simulation is used to describe the signal characteristics including the amplitude, phase and frequency distribution is a more pertinent expression. The scattering parameters usually have four parts: two-port network system: input return loss (S11), output return loss (S22), reverse isolation (S12) and forward voltage gain (S21), as shown in Figure (7). There are the import voltage signal (a1), the reflected signal (b1), and the transmitted signal into the network through amplification or attenuation after the output signal (b2) to the load. If the impedance of output port will not fully match the load, some output signal will be reflected into the network system as voltage signal (a2) generation[12].

The LNA circuit with PGS conductors has been simulated with inductive load, matching, and source degeneration, which has been designed using TSMC 0.18μm technology, and simulated by Advanced Design System (ADS2009) at 2.4GHz.

Adopting the ADS simulation software and device and process models in simulation with
TSMC 0.18μm CMOS process, the cascode LNA exhibited good performance. The circuit performance is more impressive. Here, the operating voltage of this 2.4 GHz LNA was a 1.8V supply voltage. The final simulation results show that the gain of the LNA circuit with PGS conductors enhanced from 13.14 dB to 21.474 dB as shown in Figure (6). In the PGS LNA circuit, the reverse isolation (S11) is smaller than that appear in the LNA circuit using technology inductors as shown in Figure(8).

![Graph showing gain vs frequency for LNA circuit with and without PGS.](image)

**Fig.8:** Comparison of the Gain (S21) versus frequency of LNA circuit with and without PGS.

![Graph showing reverse isolation vs frequency for LNA circuit with and without PGS.](image)

**Fig.9:** Comparison of the reverse isolation (S12) versus frequency of LNA circuit with and without PGS.

The input return loss (S11) improved from -4.489 to -7.556 dB and the output return loss (S22) also improved from -16.866 to -11.794 dB, as shown Figure (9) and (10) respectively. They have good performance. Finally, minimum noise figure performance is quite good, as shown in Figure(11).
Fig. 10: Comparison of the input return loss (S11) versus frequency of LNA circuit with and without PGS.

Fig. 11: Comparison of the output return loss (S22) versus frequency of LNA circuit with and without PGS.

Fig. 12: Comparison of the minimum noise figure nf(2) versus frequency of LNA circuit with and without PGS.
5. Comparison Between the proposed LNA With Other LNAs.
Table 1 shows a comparison between the simulation results of LNA with and without PGS. It be noticeable that the inductors with PGS improve the performance of the circuit.

Table 1: Summary of simulation results

<table>
<thead>
<tr>
<th>Parameters</th>
<th>LNA with technology inductors</th>
<th>LNA with PGS inductors</th>
</tr>
</thead>
<tbody>
<tr>
<td>S11</td>
<td>-4.489 dB</td>
<td>-7.556 dB</td>
</tr>
<tr>
<td>S12</td>
<td>-23.162 dB</td>
<td>-32.559 dB</td>
</tr>
<tr>
<td>Gain (S21)</td>
<td>13.432 dB</td>
<td>21.474 dB</td>
</tr>
<tr>
<td>S22</td>
<td>-16.866 dB</td>
<td>-11.794 dB</td>
</tr>
<tr>
<td>Noise figure NF(2)</td>
<td>3.501dB</td>
<td>2.118 dB</td>
</tr>
</tbody>
</table>

Table 2 shows the comparison of the proposed LNA with PGS inductors with the other works of LNA. It shows how the proposed LNA with PGS inductors exhibits a high impedance matching, high gain and low noise figure as compared to the other reported LNA.

Table 2: Comparison between the proposed LNA with PGS inductors and other works

<table>
<thead>
<tr>
<th>Parameters</th>
<th>[9]</th>
<th>[13]</th>
<th>[14]</th>
<th>[15]</th>
<th>Proposed LNA with PGS inductors</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF freq.( GHz)</td>
<td>2.4</td>
<td>2.4</td>
<td>3.7-4.2</td>
<td>5.8</td>
<td>2.4</td>
</tr>
<tr>
<td>S11(db)</td>
<td>-17.052</td>
<td>-12.21</td>
<td>-23.8</td>
<td>-18.9</td>
<td>-7.556</td>
</tr>
<tr>
<td>S12 (dB)</td>
<td>-13.029</td>
<td>-39.31</td>
<td>-43.5</td>
<td>-22.1</td>
<td>-32.559</td>
</tr>
<tr>
<td>Gain S21(db)</td>
<td>11.352</td>
<td>16.64</td>
<td>25.4</td>
<td>19.5</td>
<td>21.474</td>
</tr>
<tr>
<td>S22(db)</td>
<td>-21.956</td>
<td>-12.995</td>
<td>-17.5</td>
<td>-20.0</td>
<td>-11.794</td>
</tr>
<tr>
<td>Noise figure NF(2)</td>
<td>0.216</td>
<td>4.262</td>
<td>1.06</td>
<td>1.2</td>
<td>2.118</td>
</tr>
</tbody>
</table>

6. Conclusion and Contribution
In this work, a detailed study of a spiral inductor on silicon with a patterned ground shield has been presented. The effects of pattern have been demonstrated. simulated results show that the new design improves Q-factor and inductance. Upon using LNA circuit, we show that the inductors with PGS improve the performance of the circuit.

References


[12] Hsin-Chia Yang1, Ssu-Hao Peng1, Shea-Jue Wang2,b, Mu-Chun Wang1,a, Chun-Wei Lian1, Jie-Min Yang1, Hung-I Chin1, Chuan-Hsi Liu3, “High Quality of 0.18um CMOS 5.2GHz Cascode LNA for RFID Tag Applications, IEEE 2nd International Symposium on Next-Generation Electronics (ISNE) - February 25-26 , Kaohsiung, Taiwan.


تقدم هذه الورقة دراسة تفصيلية للمحاثات الحزمونية ذات الدرع الأرضي المنقوش (PGS) الذي يتم إدخاله بين المحفز ولعبة السيليكون. تم تنفيذ هذا التصميم الجديد في دائرة مضخم الضوضاء المنخفض (LNA) من نوع cascode لتحسين أداء الدائرة. تم دراسة عملية في جهد الإمداد 1.8 فولت، بنية LNA للكود الشفرة المصدر مع كل من المحاثات التقليدية وPGS في هذا الورقة، تم إضافة برنامج محاكاة Agilent ADS (نظام التصميم المتقدم) ومعلومات عملية من المعتمد TSMC 0.18μm من CMOS لتحقيق خصائص منخفضة التكامل والتكا مل العالي لتناسب مع أداء تصميم LNA 2.4 جيجاهرتز IEEE 802.11a. ووفقاً لنتائج المحاكاة المشتركة، تحسنت الكسب إلى الأمام (S21) من 83.31 إلى 18.12 ديسيبل، وكان (S12) أقل من القيمة النموذجية عند -15dB. تمثل ممانعة الإدخال (S11) ومقاومة الخرج (S22) أيضاً أداءً جيداً. بالإضافة إلى ذلك، كان أقل رقم ضجيج جيد. وبالتالي، كانت دائرة LNA مع محاثات PGS أفضل في توافر وإمكانيات مواصفات IEEE 802.11a.