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Design of High Efficient Power Amplifier with Wide-Band Input Matching Technique for UWB Wireless Applications

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ABSTRACT

The research offers the design of a highly efficient (3.1 -10.6) GHz ultra wide band (UWB) power amplifier (PA) with an improvement in the input matching, using the process of CMOS TSMC 0.065 µm. A wide input matching topology and a resistor-capacitor (RC) interstage are adopted for input matching and flatten gain improvements, respectively. The feedback circuit leading the gate inductor combined with the peaking inductive divider accomplishes a low input return loss and extends the band of operation. The post-layout simulations indicate a high flattened average power gain (S21) of 22.2 ± 1.5 dB while the improved matching topology attains a good input (S11) and output (S22) return loss below -11 dB. Moreover, a small group delay (GD) variation of ± 47.5 ps is achieved for the UWB frequencies. In addition, a great power-added efficiency (PAE) of 33% and an output power (P_{out}) of 11 dBm are achieved. The complete UWB PA design consumes only 19 mW from 1.2 supply voltage.

Keywords: Wireless Communications, Ultra-Wideband Applications, Wideband Matching, Power Amplifier

1. INTRODUCTION[1]

Ultra-Wide-band (UWB) is an attractive research issue in wireless communication fields. Communications with UWB technology offer a wide number of applications operating in a different frequency bands between 3.1 GHz to 10.6 GHz as well as their extra capacity to offer in performance and data rates [1-4]. Hence, the wideband RF front-ends design is a vital research topic. Among the transmitter front-end blocks, the power amplifier is the largest area-consuming block and the most power-hungry block [5]. Currently, CMOS technology is considered the most applicant solution for the low-cost and high-performance transceivers. However, some inherent drawbacks of CMOS, such as a low oxide breakdown voltage, that cause the CMOS PA to be the most critical block in the CMOS transceiver design [6-10].

Several topologies have been utilized in the designing of UWB amplifiers. Topologies include shunt feedback, common source-inductive degeneration, distributed amplifiers, inter-stage impedance transformer, and cascode current-reuse common source (CS) structure [11-26].

In [11], the researchers presented the cascaded configuration of two-stage amplifiers, involving resistive feedback to get a wider bandwidth and higher gain. This topology improves the input matching, but it results in a poor gain.

However, the shunt-shunt feedback [12] achieved greater gain flatness through the entire bandwidth, but the PAE is small, and the design consumes a large die-area of a chip. [13] adopted the feedback inductance to attain a flat gain through the entire band of low noise amplifier (LNA) design. It achieved a low noise figure (NF) and wide matching; besides, it consumed a low power. [14] employed the active feedback technique to improve the 1-dB compression point and attain bandwidth expansion. Inductive degeneration topology existed in [15-16] was optimized to achieve a good gain and high output power, but the matching at input and output was not as good as in the status of a resistive-shunt feedback topology, consequently, a large number of components is necessary to be required. The distributed amplifiers (DAs) topology [17] accomplished a wide matching and good gain, but they suffered from great power consumption and large die area, preventing it from being applied in low-power systems. However, the DA in [18-19] consumed a low power of only 25 mW by adopting the topology of a tapered transmission line. [20-21] employed an interstage impedance transformer between the two-staged CMOS PA to provide enough wideband interstage impedance matching and minimize the power consumption. [22], proposed the design of a two-staged UWB-PA for 3.1 GHz to 7.5 GHz. The first stage comprises of a current-reuse common gate (CG) input to expand the input matching, whereas the second stage utilizes a common source (CS) with resistive feedback to acquire a high and flat gain. [23] employed an optimized technique to acquire small group delay (GD) variation and attain a flattened gain by engaging a two-staged power amplifier; though, the design introduced a poor

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matching and low power gain. Furthermore, the current reuse technique is indeed helpful in reducing power consumption and obtaining a gain flatness, as indicated in [24-25]. However, it has a difficulty at reaching a wide range frequency band between 3.1 and 10.6 GHz [26].

In general, the design requirements of the UWB-PA, including bandwidth, output power, PAE, group delay, and linearity, decide the most suitable configuration. In this research, a small group-delay (GD) variation and a well-matched CMOS UWB PA, covering the 3.1 GHz-10.6 GHz band with great power-added efficiency (PAE) and lower power consumption for UWB wireless applications is designed, and the simulations are carried out using the TSMC 0.065 µm CMOS process. The proposed UWB PA design is composed of two stages with a recommended RC interstage for bandwidth extension and gain flatness; the first stage employs a cascode configuration with an improvement in wide input matching topology to boost the input return loss (S11) improvement, and the second power stage is utilized to booste the gain and PAE, engaging a common source (CS) configuration amplifier with a shunt peaking inductive load to expand the bandwidth. This paper is outlined as followed: Section 2 offers the circuit description and the analysis of the completed UWB-power amplifier. Section 3 outlines the simulation results and offers a comparison table of recently published researche in UWB PAs. Finally, Section 4 draws the research conclusion.

2. CIRCUIT DESCRIPTION AND ANALYSIS

A complete schematic for the UWB-PA and its small signal-equivalent circuit are offered in Figure 1 and Figure 2, respectively. It comprises a common source (CS) cascode configuration with an improved wide input matching (feedback circuit R_F, C_F leading the gate inductor L_{G1}) and a peaking inductive divider technique at the first stage; a proposed RC inter-stage; and a common source power stage. The first stage is engaged to cascode structure of M1 and M2. The cascode configuration is the most commonly used in PA topologies due to its high reverse isolation and lower power consumption. Impedance matching between M1 and M2 is essential to boost the power transfer between the two transistors. The matching between the active devices is appreciated by inserting L_1C_1 tank circuit with reasonable sizes between the transistors. Since the amplifier bandwidth is restricted because of the large capacitance of M2, a possible method of increasing the bandwidth is to add a series peaking inductive divider (L_2, L_3) at the drain of M2.

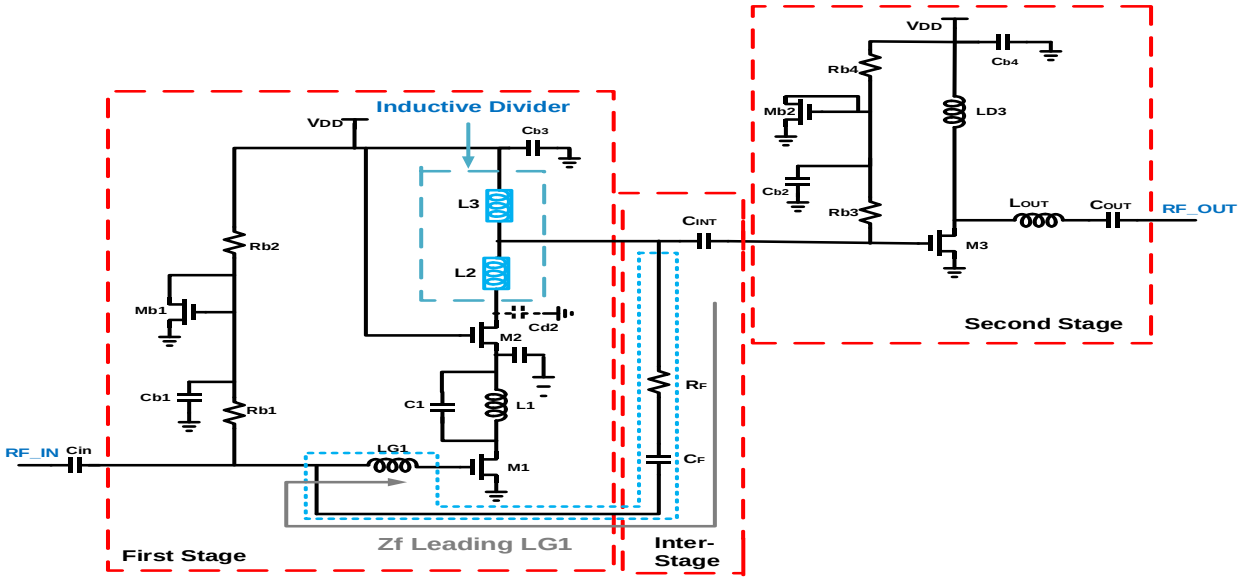

Figure 1. Complete schematic of the recommended UWB-power amplifier

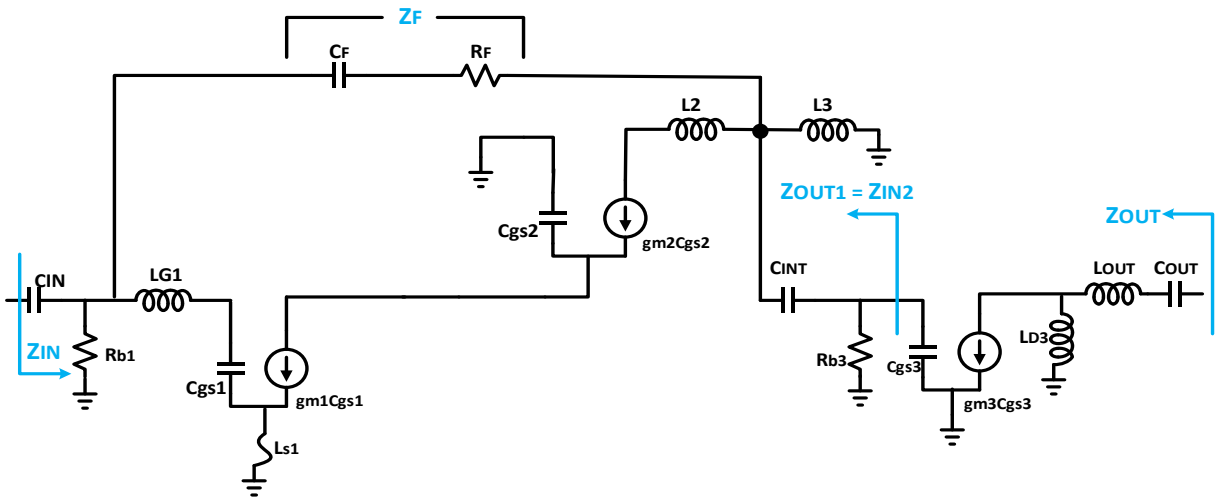

Figure 2. A small-signal equivalent circuit of the recommended UWB-power amplifier

To enrich the performance of a UWB PA in terms of a wide input matching, a recommended wide input matching enhancement technique (feedback circuit R_F, C_F leading the gate inductor L_{G1}) is suggested. The recommended matching technique is introduced in detail in section 2.1.

The output of the driver stage at transistor M2 is handed to the power stage by connecting the RC interstage circuit (R_F, C_F and C_{INT}). The interstage circuit is optimized to achieve broadband flatten gain, small group delay variation, and great power-added efficiency (PAE). The optimal value of the resistor R_F must be carefully selected to accommodate the gain and wide matching requirements. The impact of R_F on the gain flatness is demonstrated in Figure 3.

The power stage embraces the common source amplifier M3 with a shunt peaking inductive load L_{D3} to enhance the gain, maximize the PAE, and realize the small group delay variation. The network of L_{OUT} and C_{OUT} is adopted to boost the broadband output matching across the whole bandwidth.

Bypass capacitors C_{b1} to C_{b5} behave as a short circuit at high frequencies and discard the influence of noise from the power supply. The biasing circuits formed by (M_{b1}, R_{b1}, and R_{b2}) and (M_{b2}, R_{b3}, and R_{b4}) are employed to bias M1 and M3 transistors, respectively. Table 1 gives the size of the recommended PA design parameters.

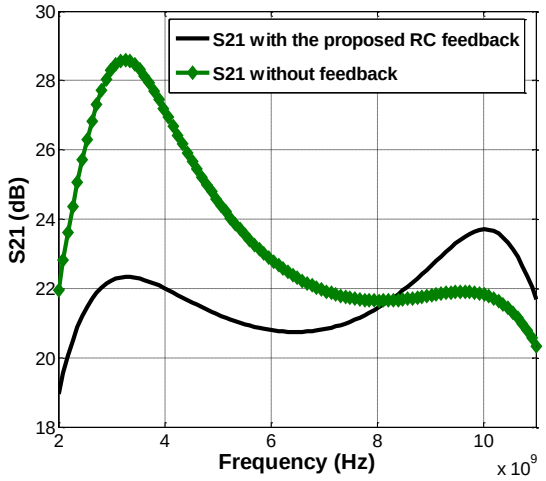

Figure 3. Influence of the shunt feedback (R_F and C_F) on the gain flatness of the recommended UWB-PA

Table 1. Parameter values of the recommended UWB PA

Design parameter	Values	Design parameter	Values
M1	L=60 nm,W=100 μm	L_1	186 pH
M2	L=60 nm,W=50 μm	L_2	250 pH
M3	L=60 nm,W=160 μm	L_3	6.3 nH
C_{IN}	5 pF	L_{OUT}	755 pH
C_1	200 fF	L_{D3}	4.3 nH
C_{INT}	1.5 fF	R_F	500 Ω
C_F	1 pF	R_{b1}	100 Ω
C_{OUT}	1.5 pF	R_{b2}	400 Ω

L_{G1}	1.8 nH	R_{b3}	700 Ω
M_{b1} / M_{b2}	L=0.06 μm, W=60 μm	R_{b4}	400 Ω

2.1 Wide-Band Input Impedance Matching

A wide-well input-matched PA is vital to accomplish a great gain. A widely used wide input matching as displayed in Figure 4 (A), uses the resistive-capacitive feedback that is adopted in most PAs. By ignoring the miller effect of the gate to drain capacitance C_{gd}, the total input impedance of a regular matching circuit (R_F, C_F lagging gate inductor L_{G1}), without the inductive divider technique can be formulated as Equation (1), where g_{m1} and C_{gs1} are the transconductances and the gate to the source- parasitic capacitance of M1 transistor, respectively.

$$Z'_{in} = \frac{1}{SC_{IN}} + SL_{G1} + [\, Z'_{F\_in} // \, (\frac{1}{SC_{gs1}} + \frac{g_{m1}}{C_{gs1}} L_{s1} + SL_{s1})] \quad (1)$$

To additionally boost the input reflection coefficient, shunt feedback with a bandwidth enrichment technique (feedback circuit R_F, C_F leading gate inductor L_{G1} combined with a peaking inductive divider (L_2, L_3)) is suggested in the design, as shown in Figure 4 (B), the input impedance (Z_{in}) of the recommended circuit is written as $Z_{in} = Z_g // Z_{F\_in}$, where Z_g is the input impedance of the amplifier without the feedback circuit, and Z_{F_in} is the impedance considering the feedback impedance Z_F. The impedance Z_g can be derived as Equation (2), and the L_{G1}, L_{s1}, and C_{gs1} are determined by Equations (3)-(4).

$$Z_g = \frac{1}{SC_{gs1}} + S\,(L_{G1}+L_{s1}) + \frac{g_{m1}}{C_{gs1}} L_{s1} \quad (2)$$

where g_{m1} is the M1 transconductance and C_{gs1} is the parasitic capacitance between the gate and the source terminals of the M1 device. Furthermore, the inductors L_{s1} and L_{G1} are chosen to resonate with C_{gs1} to cancel the imaginary part of the input impedance. Giving the imaginary part of (2) to nil, the resonance frequency can be formulated as,

$$f_{o1} = \frac{1}{2\pi\sqrt{C_{gs1}(L_{G1} + L_{s1})}} \quad (3)$$

At matching, the input impedance of the PA is equal to Z_o, the impedance of the source. Setting the real part of (2) to Z_o, L_{s1} is derived as,

$$L_{s1} = \frac{Z_o\, C_{gs1}}{g_{m1}} \quad (4)$$

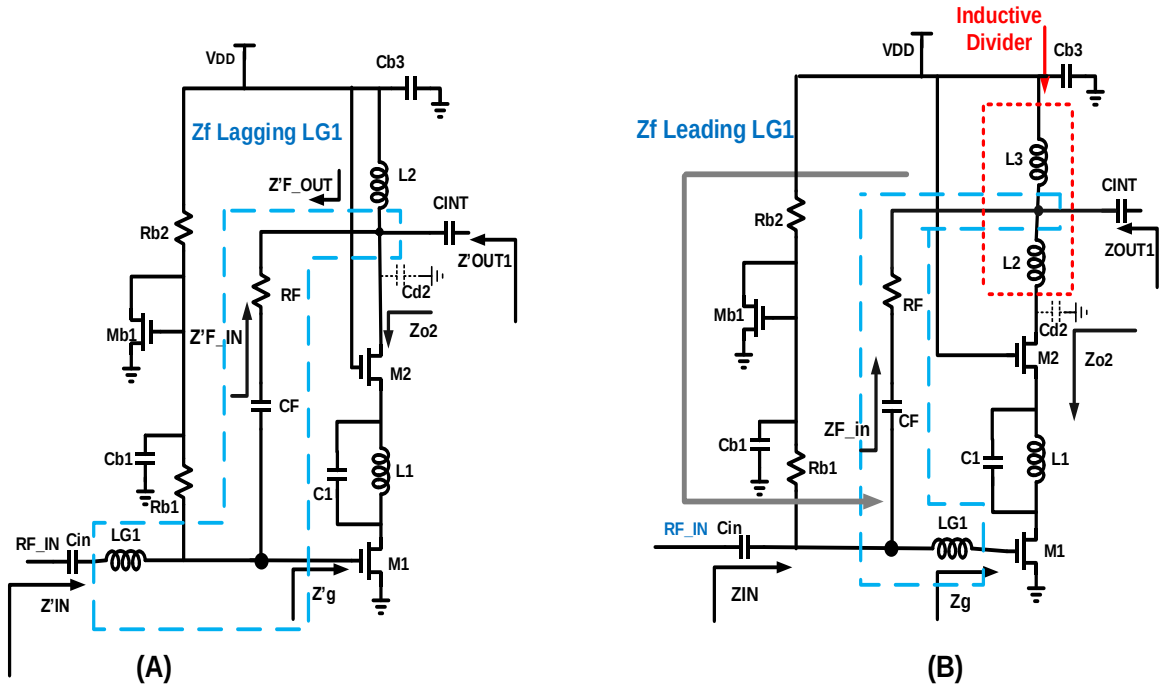

Figure 4. A circuit with wideband input matching topologies (A) a regular matching with feedback circuit (Z_F lagging the gate inductor L_{G1}) without the inductive divider, and (B) a proposed wideband input matching topology (feedback circuit Z_F leading the gate inductor L_{G1}) combining with the peaking inductor divider

Therefore, the inductance of L_{s1} can be calculated by the parameters g_{m1}, C_{gs1}, and Z_o.

The impedance Z_{F_in} can be expressed as Equation (5):

$$Z_{F\_in} = \frac{R_F + [SL_2 \,//\, (SL_3 + \frac{1}{SC_{d2}})]}{1 + \frac{g_{m1}\,[SL_2 \,//\, (SL_3 + \frac{1}{SC_{d2}})]}{[S^2C_{gs1}(L_{G1}+L_{s1}) + sg_{m1}L_{s1} + 1][S^2C_{d2}(L_2 + L_3) + 1]}} \quad (5)$$

where C_{gs1} and C_{d2} are the parasitic capacitors. In a usual design, $S^2C_{gs1}(L_{G1} + L_{s1}) + sg_{m1}L_{s1} \ll 1$, $S^2C_{d2}(L_2 + L_3) \ll 1$, and $g_{m1}\,[SL_2 \,//\, (SL_3 + \frac{1}{SC_{d2}})] \gg 1$, are satisfied. Therefore, the formula of Z_{F_in} in Equation (5) can be approximated by Equation (6),

$$Z_{F\_in} = \frac{R_F}{g_{m1}\,[SL_2 \,//\, (SL_3 + \frac{1}{SC_{d2}})]} + \frac{1}{g_{m1}} \quad (6)$$

Giving the imaginary part of (6) to zero allows calculating the resonance frequency f_{o2} of the proposed circuit in Figure 4 (B) as follows,

$$f_{o2} = \frac{1}{2\pi\sqrt{C_{d2}(L_2 + L_3)}} \quad (7)$$

Considering (2) and (6), the overall input impedance (Z_{in}) of the proposed technique shown in Figure 4(B) can be derived as Equation (8),

$$Z_{in} = Z_g \,//\, Z_{F\_in} \quad (8)$$

Figure 5 plots the simulated input return loss (S11) with respect to frequency for Z'_{in}, the regular matching circuit in figure 4 (A), and ($Z_{in} = Z_g \,//\, Z_{F\_in}$) of the proposed matching circuit in figure 4 (B). As seen in Figure 5, the wideband input matching can be effectively realized by introducing a pole of frequency f_{o2}, and it is noticed that the suggested input matching circuit (feedback circuit R_F, C_F leading the gate inductor L_{G1} and combining with the peaking inductive divider) realizes a better input return loss across the 3.1 to 10.6 GHz band than the conventional matching circuit (feedback circuit lagging the gate inductor L_{G1}).

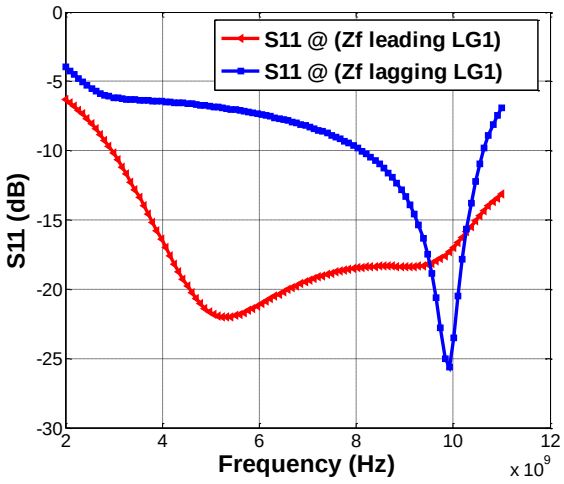

Figure 5. Simulated input return loss (S11) with respect to frequency for $Z_{in}(= Z_g // Z_{F\_in}; Z_F$ leading $L_{G1})$ of the suggested topology in Figure 4 (B), and Z'_{in} (; Z_F lagging L_{G1}) of the regular topology in Figure 4 (A)

2.2 Inter-stage Impedance matching

In the two-staged PA design, the output impedance of the driver stage (first stage) Z_{out1} symbolizes the source impedance of the power stage (second stage) Z_{in2}. To boost the PAE, the output impedance of the driver stage must follow the locus of maximum PAE in the power stage. Therefore, as shown in Figure 6, a wideband interstage impedance transformer formed by the proposed RC circuit (R_F, C_F, and C_{INT}) is employed. As outlined in Equation (9), the driver stage output impedance Z_{out1} after the interstage matching, (R_F, C_F, C_{INT}, R_{b3}, and L_3) is carefully optimized to match the first stage output impedance Z_{out1} to the optimal source impedance of the power stage Z_{in2}.

$$Z_{out1} = Z_{in2} = R_{b3} //[\frac{1}{SC_{INT}} + (SL_3 // Z_f)] \quad (9)$$

$$Z_{out1} = R_{b3} // \frac{S^2 Z_f L_3 C_{INT} + SL_3 + Z_f}{S^2 L_3 C_{INT} + SC_{INT} Z_f} \quad (10)$$

$$Z_f = \frac{R_F + 1/SC_F}{1 + 1/A_{v1}} \quad (11)$$

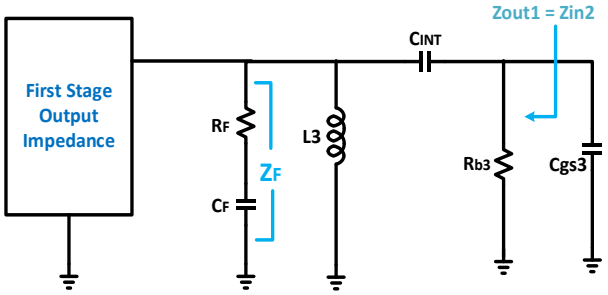

Figure 6. Small-signal equivalent circuit for the interstage matching

2.3 Output matching

A series resonant circuit consisting of the capacitor C_{out}, and the inductor L_{out} along with the inductor L_{D3} is playing the role of the output impedance matching circuit. Figure 7 indicates the output impedance small-signal equivalent circuit. The inductor L_{out} along with the capacitor C_{out} and L_{D3} should be optimized for achieving a small GD variation and improving the PAE. The output impedance can be outlined by Equation (12),

$$Z_{OUT} = SL_{D3} + \frac{1}{SC_{OUT}} + SL_{OUT} \quad (12)$$

$$Z_{OUT} = \frac{S^2 L_{D3} C_{OUT} + S^2 L_{OUT} C_{OUT} + 1}{SC_{OUT}} \quad (13)$$

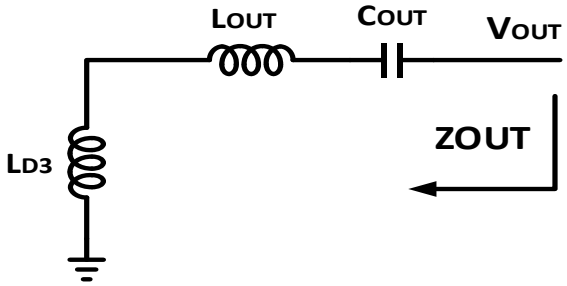

Figure 7. Small-signal equivalent circuit for the output impedance

3. SIMULATION RESULTS AND DISCUSSIONS

The proposed 3.1 GHz - 10.6 GHz UWB-PA is designed and simulated using the 0.065 µm TSMC CMOS process with a Cadence tool in a post-layout level, within a 1.2 supply voltage.

Figure 8 presents the layout of the proposed PA. The total size occupied by the PA is 0.95 mm × 1.3 mm; inductors and capacitors are occupying the largest percentage of the area.

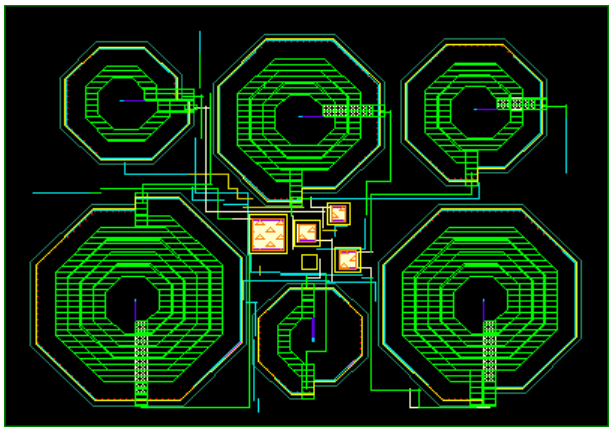

Figure 8. The layout of the recommended UWB PA

Figure 9 offers the S-parameters simulation results of the input and output return loss. As displayed in Figure 9, the proposed PA has (S11) and (S22) of less than -11dB, over the whole frequency band. The input return loss (S11) simulation results illustrate the improvements in the wideband input impedance match while the output return loss (S22) simulation results demonstrate that the series output matching circuit matches the load well to 50 Ohms.

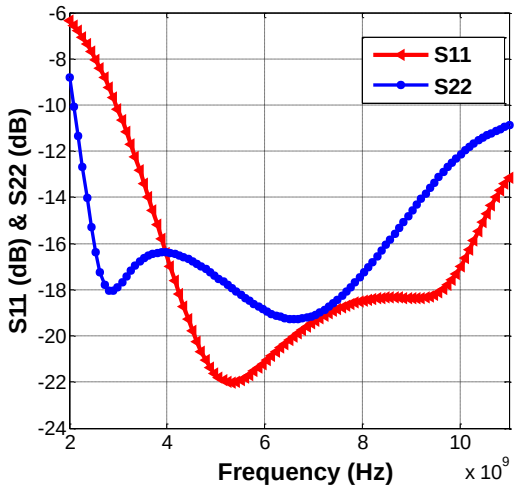

Figure 9. Simulation results of the input return loss (S11) and the output return loss (S22)

To enhance the gain of the first stage, a peaking technique is suggested that helps in attaining a high and flat gain. In addition to the contribution of shunt resistive-capacitive feedback topology in the stabilization of the amplifier, the resistive-capacitive feedback topology contributes to gain flatness. From the post-layout simulation, as shown in Figure 10, the proposed UWB-PA can attain a high power gain of 22.2 ± 1.5 dB over 3.1 GHz – 10.6 GHz frequency band.

The proposed UWB PA can be considered a unidirectional amplifier since its reverse isolation coefficient (S12) is below -50 dB, across the entire frequency band, as shown in Figure 10.

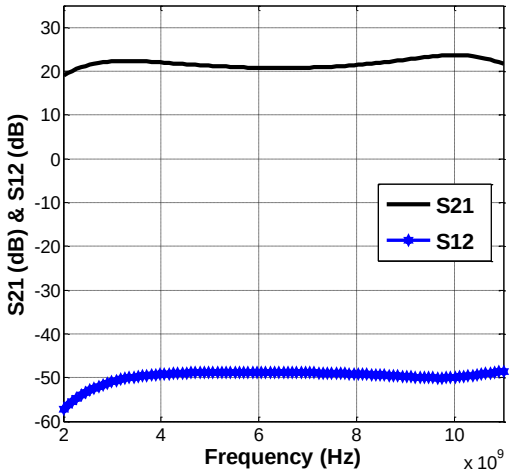

Figure 10. The simulation results of the power gain (S21) and the reverse isolation (S12)

Group delay (GD) is a key criterion to estimate the power amplifier phase nonlinearity. In a wideband communication, the GD variation must be held low for a better phase linearity since the large variation in GD involves more phase distortion, and the output does not maintain its original input. As illustrated in Figure 11, a small group delay variation of ± 47.5 ps is accomplished through the interested frequency band.

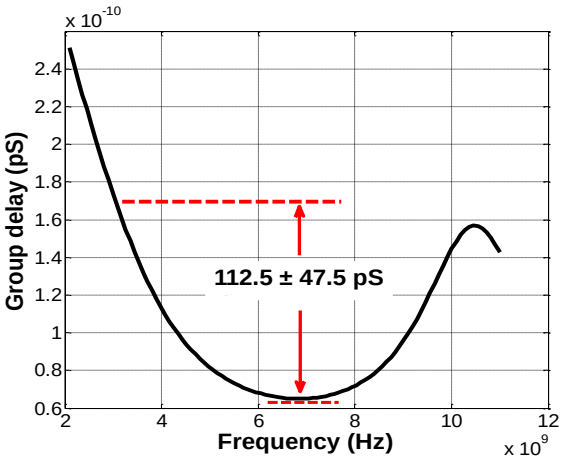

Figure 11. Group delay (GD) simulation result

In addition, the recommended UWB-PA attains a maximum PAE of 33 %, 28.5 %, 25.7 %, and 20.8 % at 4 GHz, 6 GHz, 8 GHz, and 10 GHz, respectively, as displayed in Figure 12. The PAE is a crucial parameter that measures the PA performance, and it is boosted by enhancing the input, output, and inter-stage matching.

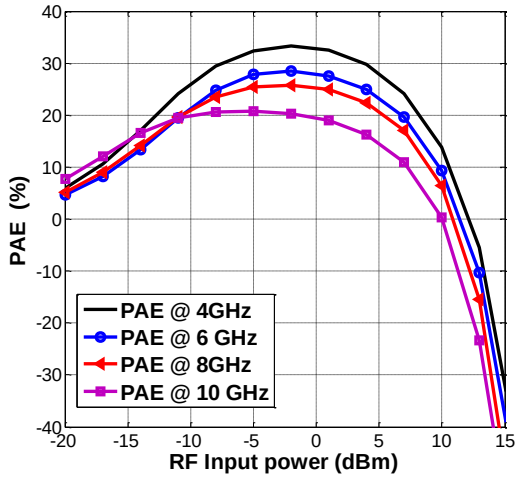

Figure 12. Simulation results of the power added efficiency (PAE)

Moreover, the power amplifier attains an output power (P_{out}) of 11.5, 11 dBm, 10.5 dBm, and 10 dBm at 4 GHz, 6 GHz, 8 GHz, and 10 GHz, respectively, as given in Figure 13.

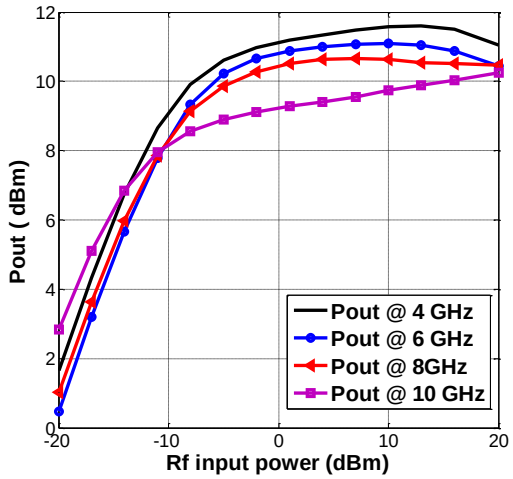

Figure 13. Simulation results of the output power (P_{out})

Finally, the UWB-PA consumes a low power consumption of 19mW and is unconditionally stable, as presented in Figure 14, over the whole frequency band.

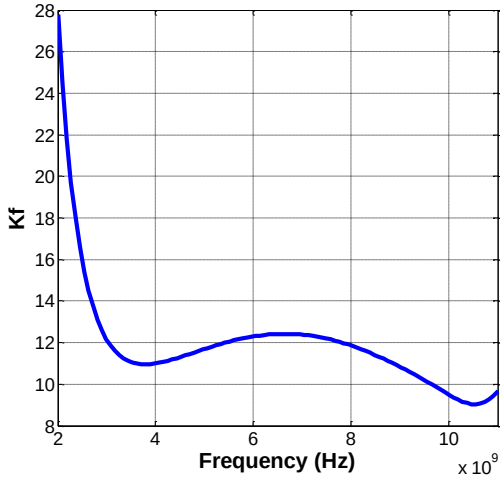

Figure 14. Simulation result of the stability factor (Kf)

Table 2 outlines a simple comparison between the performance summary of the recommended UWB PA with the recently published researche on UWB PAs in CMOS technology. As it can be concluded from the table, the proposed PA has the best performance in terms of matching behavior and power-added efficiency; in addition to a small group delay variation, lower power consumption and a great flatten gain through the full band.

4. CONCLUSION

The paper presents a methodology to design a wide band power amplifier (PA) for UWB wireless applications using the TSMC CMOS 0.065 µm technology. The proposed UWB-PA uses a new topology for wide input matching (feedback circuit R_F, C_F leading the gate inductor L_{G1}) based on a cascode common source topology with a peaking inductive divider (L_2, L_3) for a bandwidth enhancement. Inductive peaking at the power stage is used to flatten and increase the PA power gain. This UWB PA achieves a well wideband input and output impedance matching, a small GD variation, a high PAE, and a high and flat power gain with high reverse isolation over the operating frequency band (3.1 GHz – 10.6 GHz).

Table2. Post-layout-simulation results of the recommended UWB-PA in comparison to recent researche in CMOS UWB-PA

Ref.	CMOS Technology (nm)	Frequency (GHz)	Gain (dB)	S11 (dB)	S22 (dB)	Dissipated Power (mW)	GD (ps)	PAE (%)	OP1dB (dBm)	Area (mm^2)
[27]	180	3-7	19 ± 0.3	< -7.5	< -6	28	± 200	29	8.2	0.749
[28]	180	2.8-5.2	16.2 ± 0.4	< -6	< -0.5	25	± 70	47	10.1	N/A
[29]	130	6-9	9 ± 1	< -8	< -9	24	N/A	22	7	0.86
[30]	180	3.1-10.6	12.5 ±1.5	< -4.5	< -8.5	36	± 50	32.5	11	0.55
[31]	65	3.1-10.6	22.8 ± 1.2	< -7	< -10	15.5	± 50	29.5	6.8	1.17
[32]	180	3.1-10.6	28.7 ± 2	< -10.5	< -13.7	23	± 60	33	5.6	N/A
This work	65	3.1-10.6	22.2 ± 1.5	< -11	< -11	19	± 47.5	33	6.14	1.2

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