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A 3.1-10.6 GHz Hybrid Class-F Class-E Power Amplifier

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***Abstract*—A hybrid class-F-class-E power amplifier (PA) with proposed inductor-capacitor (LC) interstage was designed and simulated using130-nm CMOS technology. The driver stage (class-F) is employed to operate as a switch to improve the efficiency of the designed UWB-PA. The proposed inductor-capacitor (LC) inter-stage is used to improve the linearity of the proposed PA. The class-E PA is used as the main stage to enhance gain and output power. The proposed circuit operates in the ultra-wideband band from 3.1 GHz to 10.6 GHz. The designed circuit achieves a 26.4-dBm output power, a power added efficiency (PAE) of 54%, an output referred IP3 (OIP3) of greater than 33-dBm and a 27-dB maximum gain. Moreover, the circuit realized ±44 ps group delay variation . The proposed circuit satisfies the need for class-E amplifiers with fast input exchange signals, such amplifiers are required to realize zero voltage and zero derivative switching (ZVDS) without adding a large dissipation, which is achieved via the use of a class-F PA as the driver stage. This circuit provides high PAE and good linearity.**

Keywords— Class-F, Class-E, power amplifier, linearity and power-added efficiency

I. Introduction

The heavy usage of cellular 4G has made the notion of 5G an attractive business proposition. As the first release of the 5G standard is approaching, leading operators worldwide are preparing for their initial 5G launch. Because the 3.5 GHz band (3.3 GHz-3.8 GHz) will be the dominant mid-band choice for these early 5G deployments, its coverage capability will have a big influence on the strategy choice of the 5G operators. The power amplifier (PA) proposed in this work is designed to be used as the last stage in the transmitter for 5G at 3.5 GHz. Class-E PAs have been widely utilized within Wi-Fi communications owing to their simple circuits and high efficiency. One of the main problems in the class-E PA is obtaining the input signal. We must apply a square signal to switch the PA from the on state to the off state and vice versa in order to reduce the transition time. Logic gates are usually used to generate such a waveform at high frequencies, but that method leads to large power dissipation [1]. To solve this problem, input frequency harmonics are generated and combined to produce a square wave signal. This can be done by using a class-F power amplifier configured with a tuned LC parallel tank. The class-F PA has zero impedances at even-order harmonics and infinite impedances at odd-order harmonics ,which creates half-sinusoidal current and square voltage [2]. The first tuned LC tank is adjusted to be at the first harmonic of the input frequency, and the other is tuned to the third harmonic [1]. This process will produce the voltage of the drain with the essential first and third harmonic signal. This can be used as an approximation of a square wave signal. This signal will be applied to the input of a class-E PA to avoid long transition times. The usage of the class-F PA driver stage increases the PA efficiency but reduces the linearity of the Class-E PA, for this reason, inductor-capacitor (LC) inter-stage circuit is used to improve the linearity of the PA.

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II Driver Stage Class-F PA

Class-F PAs have been utilized to increase the efficiency and the output power of class-E PAs. This can be achieved by using multiple odd harmonic resonators LC tanks in the output network, as shown in figure (1). Using multiple odd harmonic resonators provides high impedance at the PA drain, which results in a small current. This process ensures only voltage signal will appear at odd harmonics and only Current signal will appear at even harmonics. Thus, the drain current and the drain voltage waveforms are created without any overlap between them. This technique yields high efficiency and low power consumption, which also reduces the need for extra filtering and the harmonic power can be reduced. Another configuration that can be used to realize a class-F PA is displayed in figure (2).The L_1-C_1 that resonates at the second harmonic gets to be inductive load at the third harmonic, and the L_2-C_2 that resonates at the fourth harmonic gets to be capacitive load at the third harmonic. As a result, the parallel equivalent inductor and capacitor have a third harmonic resonance. Hence, the impedance of the third harmonic becomes very high, which helps to improve the operation efficiency of the class-F PA [3]. In an ideal case,, the signal of the voltage should be close to a square signal and the signal of the current should be close to a half sine signal as shown in figure (3). There is no overlap between the drain current and drain voltage, so the power dissipation over the transistor is reduced, driving with 100% efficiency [4].

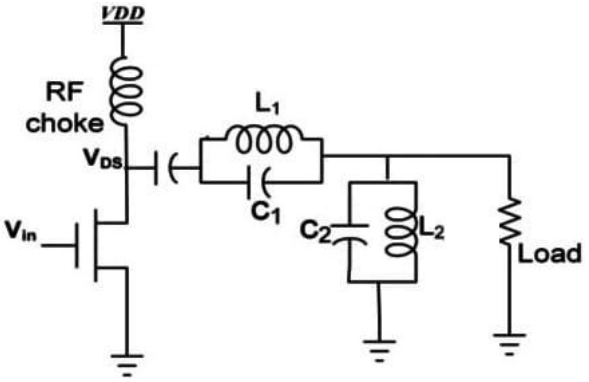

Figure 1 Schematic of a class-F PA

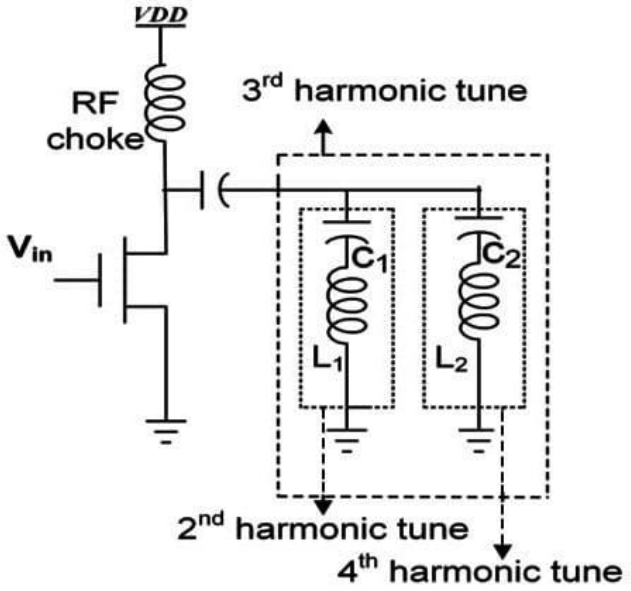

Figure 2. The configuration used to achieve a class-F PA.

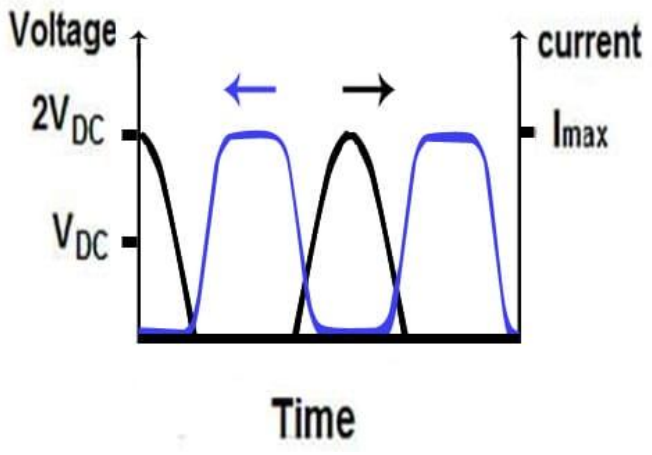

Figure 3. Class-F PA voltage and current signals[4].

The V_{DS} of the class-F PA with odd harmonics can be composed according to,

$$V_{DS} = V_{DD} - V_m \cos(\omega_o t) + \sum_{n=3,5,7,\ldots}^{\infty} V_{mn} \cos(n\omega_o t) \quad (1)$$

where V_{DD} is the voltage of the supply, V_m is fundamental component of the drain voltage, V_{mn} is the amplitude of n-th harmonic of V_{DS}, and ω_o is the angular frequency at the operating frequency. The drain current i_D is given by,

$$i_D = I_{DD} + I_m \cos(\omega_o t) + \sum_{n=2,4,6,\ldots}^{\infty} I_{mn} \cos(n\omega_o t) \quad (2)$$

where I_{DD} is the DC current from V_{DD}, I_m is the drain current of the basic component, and I_{mn} is the amplitude of n^{-th} harmonic of i_{DS} [3]. We see from equations (1) and (2) that there is no power at the harmonics of the system because there is no current or voltage displayed at the same harmonic frequency as the drain voltage wave displayed at the odd harmonics and the drain current wave displayed at the even harmonics [5].

III Inductor-Capacitor(LC) Interstage

One drawback of the class-E PA is its low linearity characteristics. Nonlinearity can be defined as the existence of higher-order harmonics; the inductor-capacitor(LC) inter stage, which operates as an integrated passive predistortion linearizer, produces an anti-phase between the input and the output signals, which cancels out the unwanted signals generated by the PA. From Figure 4, the PA's input and output voltages can be given as follows[6]:

$$v_{out} = a_0 + a_1 v_b + a_2 v_b^2 + a_3 v_{b,}^3 \quad (3)$$

$$v_b = b_0 + b_1 v_{in} + b_2 v_{in}^2 + b_3 v_{in}^3. \quad (4)$$

While the fundamental, second, and third harmonics of the voltages V_b and V_{in}, respectively, are represented by the coefficients $a_{1,2,3}$ and $b_{1,2,3}$. The D.C components are a_0 and b_0, and the output voltage is V_{out} while the gate voltage is V_b. By substituting Equation (4) into Equation (3) and considering the third-order components and fundamentals, we have

$$V_{out} = a_1(b_1 v_{in} + b_3 v_{in}^3) + a_3(b_1 v_{in} + b_3 v_{in}^3)^3$$

$$= a_1 b_1 v_{in} + (a_1 b_3 + a_3 b_1^2) v_{in}^3 + 3a_3 b_1^2 + 3a_3 b_3^2 b_1 v_{in}^7 + a_3 b_3^3 \quad (5)$$

To cancel out the part of the third order components:

$$a_1 b_3 + a_3 b_1^3 = 0 \quad (6)$$

$$b_3 = -\frac{a_3 b_1^3}{a_1} \quad (7)$$

By setting the fundamental amplitudes of a1 and b1 to 1, we have

$$b_3 = -a_3 \quad (8)$$

The PA's third intermodulation distortion (IMD3) will be cancelled by Equation (8). So we used the proposed inter-stage circuit which is formed by L_6, C_5 and C_6 between the class-F stage and the class-E stage for this purpose. Therefore, the linearity of the circuit is improved. To improve (GD) variations, the values of L_6, C_5, and C_6 are adjusted several times simultaneously, L_6, C_5, and C_6 values are enhanced and proposed to be 1.8nH, 1.2pf, and 1pf respectively. Figure 5 shows the effect of the inductor-capacitor (LC) inter-stage on the group delay (GD) variations.

III. Main Stage Class-E PA

The class-E PA operates at very high operating frequencies, contingent on the value of the output capacitance necessary for the output-matching network [7]. At very high frequencies, the capacitance C_s limits the maximum efficiency. Figure (6) shows the basic configuration of the class-E PA that comprises a transistor, which is used as an active switch and a capacitor C_p which acts as a connected shunt with the transistor to obtain the zero voltage switching (ZVS) and zero-derivative switching (ZDS) situations of the class-E PA [8]. (ZVS/ZDS) situations exhibit low noise, zero switching loss, and they improve the constituent tolerances required for soft switching. An inductor L_p is used to ensure the current I_{DC} of the supply is constant DC (it is of infinite impedance). Given a desired output power, the required value of R_E can be calculated as,

$$R_E = \frac{0.577(V_{DD} - V_{knee})^2}{P} \qquad (9)$$

where R_E is the optimum load resistance, V_{DD} is the drain voltage, and V_{knee} is the knee voltage of the CMOS transistor. The series load network is adjusted to a value below the fundamental frequency f_o to give the right inductive load at f_o in order to obtain the operation of the class-E PA with high efficiency. The output network load quality factor Q_L is defined as [9].

$$Q_L = \frac{2\pi f_o L_o}{R_E} \qquad (10)$$

The tuning tank theoretical values can be calculated from,

$$L_p = \frac{R_E Q_L}{2\pi f_o} \qquad (11)$$

$$C_p = \frac{1}{2\pi f_o (Q_L - 1.152)} \qquad (12)$$

V. The Proposed Class-E PA

The complete proposed circuit is shown in Figure 7, where the proposed circuit contains three main stages. The first stage is the class-F PA (driver stage), which is used to generate a square signal to turn the class-E PA from the on state to the off state and vice versa. This is used rather than logic gates, which avoids large power consumption and therefore increases the efficiency. The second stage is The proposed inductor-capacitor (LC) inter-stage which is used to produce an inverse phase response between the input voltage and the output voltage of the PA. Therefore, the PA's third intermodulation distortion (IMD3) will be zero. This procedure decreased GD variations, which improved the circuit linearity. The third stage is the class E PA which is used as the main PA as it has properties that simultaneously improve the linearity and achieve wideband input matching.

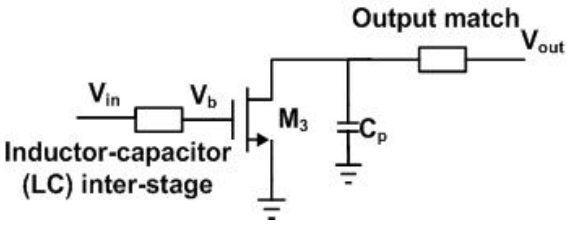

Figure 4. Concept analysis of inductor-Capacitor (LC) inter-stage on the PA.

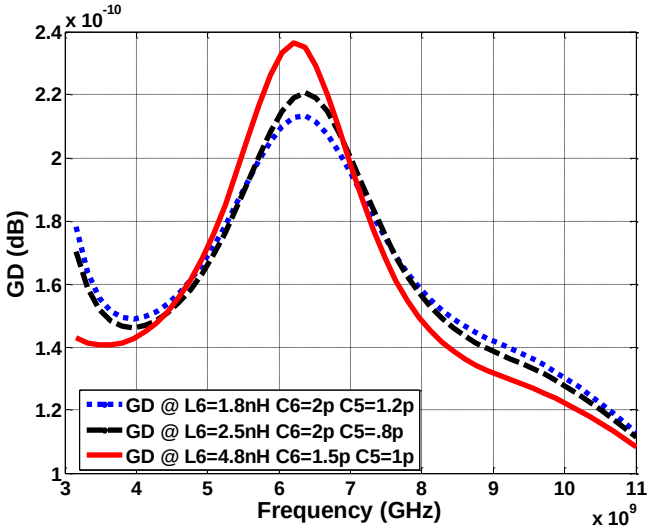

Figure **5.** Effect of L_6, C_5 and C_6 on group delay variation.

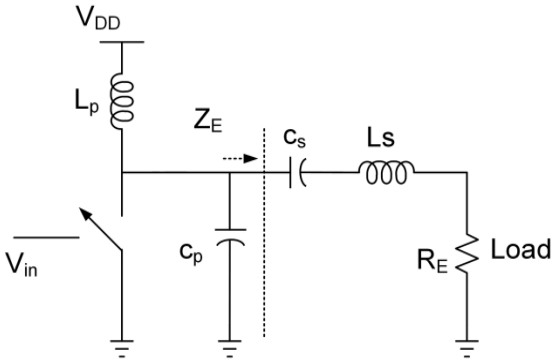

Figure 6. Class-E PA schematic.

IV. Matching Of The Proposed Circuit

The output network consists of a matching circuit that acts as a low-pass filter that matches the output. As displayed in figure 8, the output impedance of the driver stage (the class-F PA) is the input impedance of the main stage (the class-E PA). We employed the shunt and series resonance circuits to force the output impedance of the class-F PA to follow the optimum input impedance of the class-E PA in order to get sufficient power added efficiency (PAE) through the band.

$$Z_{in} = \frac{1}{SC_1} + R_{b2} \quad (13)$$

$$Z_{in} = \frac{1+SC_1R_{b2}}{SC_1} \quad (14)$$

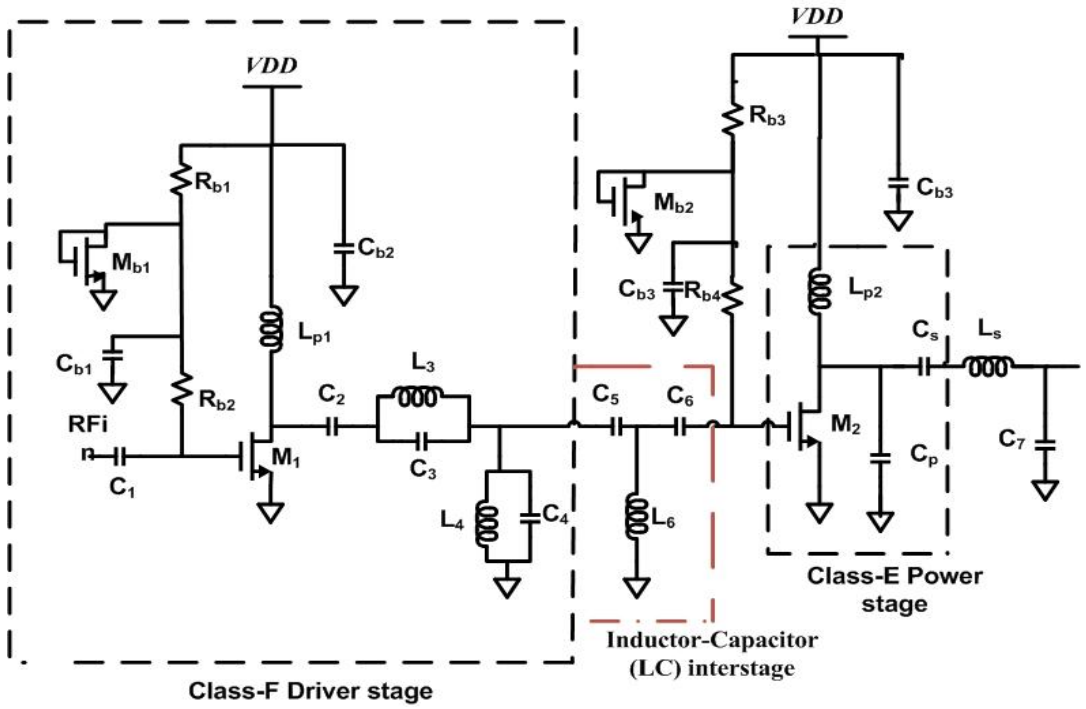

Figure 7. The proposed Hybrid Class-F class-E power amplifier

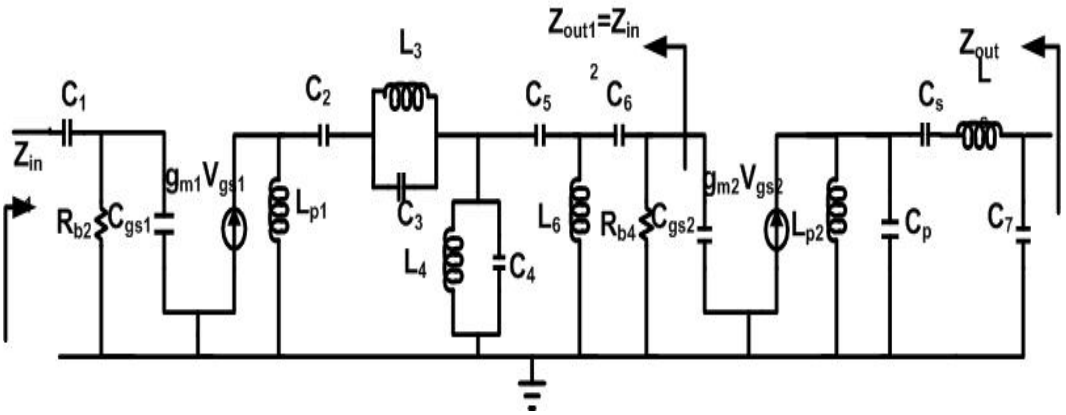

Figure 8. Equivalent circuit model of the Proposed Hybrid Class-F class-E power amplifier.

$$Z_{out1} = Z_{in2} = \left[\left[\left[\left[SL_{p1} + \frac{1}{SC_2} + \left[SL_3 /\!/ \frac{1}{SC_3}\right]\right] /\!/ \left[SL_4 /\!/ \frac{1}{SC_4}\right]\right] + \frac{1}{SC_5}\right] /\!/ SL_6\right] + \frac{1}{SC_6}\right] /\!/ R_{b4} \quad (15)$$

$$Z_{out1} = Z_{in2} = \left[\left[\left[\left[SL_{p1} + \frac{1}{SC_2} + \left[\frac{SL_3}{S^2L_3C_3+1}\right]\right] /\!/ \frac{SL_4}{S^2L_4C_4+1}\right] + \frac{1}{SC_5}\right] /\!/ SL_6\right] + \frac{1}{SC_6}\right] /\!/ R_{b2} \quad (16)$$

$$Z_{out} = \frac{1}{SC_7} /\!/ \left[SL_s + \frac{1}{SC_s}\right] + \left[SL_{p2} /\!/ \frac{1}{SC_p}\right] \quad (17)$$

$$Z_{out} = \frac{1}{SC_7} /\!/ \left[\frac{S^2L_sC_s + 1}{SC_s}\right] + \left[\frac{SL_{p2}}{S^2L_{p2}C_p + 1}\right] \quad (18)$$

IIV. RESULTS

The Cadence Spectre simulator is used to simulate the proposed circuit using TSMC 130-nm technology. The PAE is an important measure for determining the PA's performance. therefore the PAE is enhanced by using Class-F. The simulation of PAE as a function of input power at three different frequencies within UWB is plotted in figure 9. The proposed circuit achieved a good PAE of 51.5% at 8GHz ,35% at 10GHz and 22% at 6GHz, which is considered a good PAE that is stable for the application where the size of the battery is crucial, as a larger battery size is not required as a result of the increased circuit efficiency. The PAE as a function of frequency are plotted in Figure 10 across the band from 3 to 11 GHz. The PAE is maximum at 8GHz and has good results for the range from 6.2 GHz to 10 GHz.

Figure 11 shows the results of a simulation the output power versus the input power signal at three different frequencies across the operating bandwidth. The simulation output power is 26 dBm at 8G, 25 dBm at 10G, and 19 dBm at 6G . As displayed, the output power increases rapidly with low input power and reaches to saturation after a few input powers, Which is a good performance. The power output from the UWB transmitters needs to be not high to avoid interfering with the communication networks that are already in existence within the UWB .Also, The output power as a function of frequency is plotted in Figure 12 across the band from 3 to 11 GHz. The output power is maximum at 8 GHz and still approximately constant till 11 GHz.

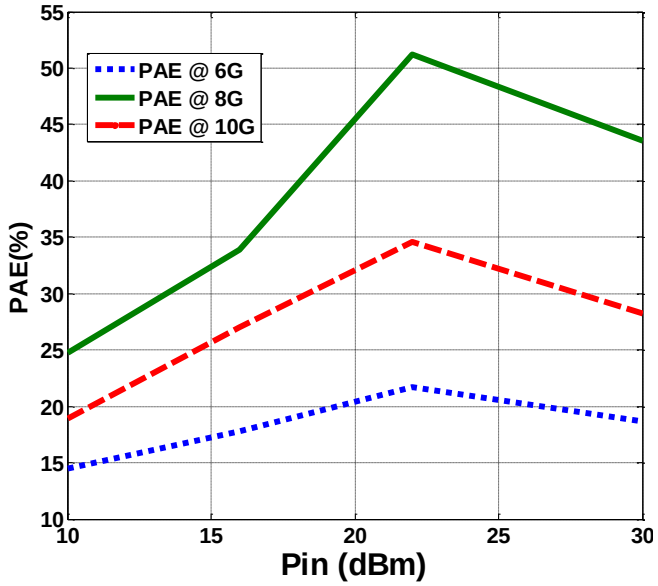

Figure 9. the Simulation of PAE at three different frequencies.

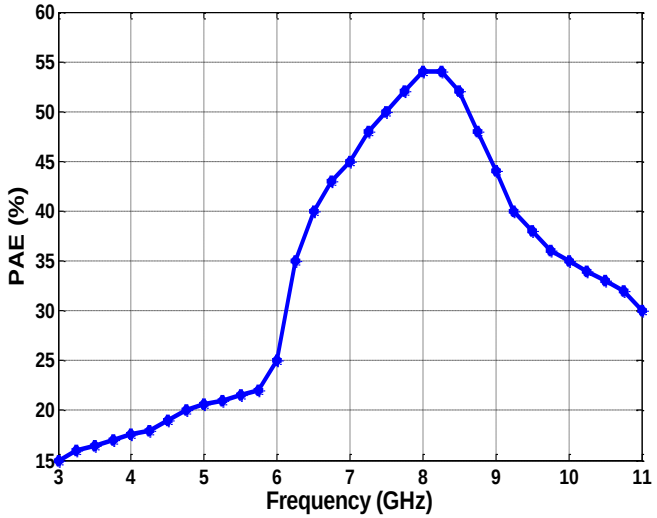

Figure 10. the Simulation of PAE as a function of frequency.

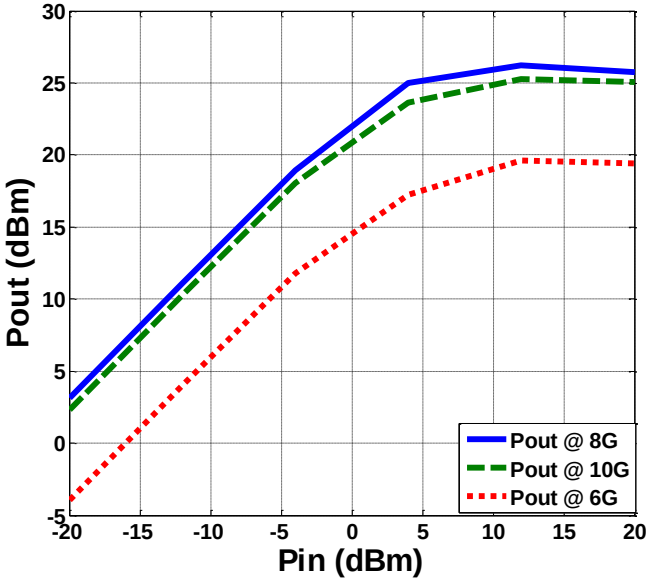

Figure 11. the Simulation of output power at three different frequencies.

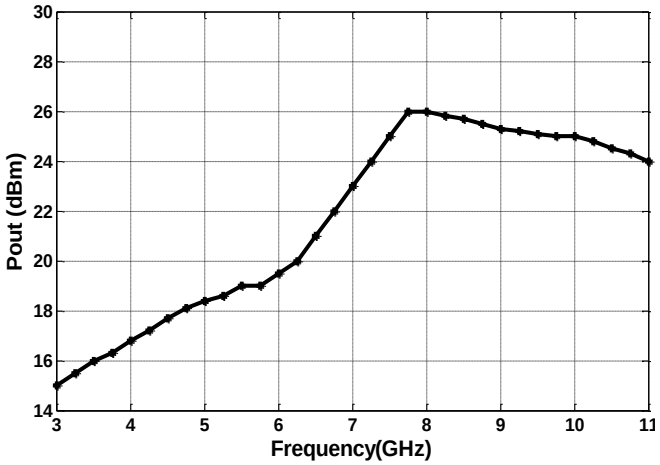

Figure 12. the Simulation of output power as a function of frequency.

Another crucial measure for any amplifier is the linearity. The term "linearity" describes the linear alteration of the PA's output power with respect to input power. Figure 13 shows the output-referred IP3 (OIP3) after and before the use of an inductor-capacitor (LC) inter-stage circuit, which demonstrates how the linearity of the circuit improved after using an inductor-capacitor (LC) inter-stage circuit. In Figure 14, the UWB S-parameter of proposed PA's circuit is illustrated. The average S21 is 24 dB which achieved high gain and S12 is smaller than -42dB which has a good isolation. As a result of forcing the output impedance of class F to follow the optimum input impedance of class E and using the broadband matching network at the output, S11 and S22 are less than -10 dB of the entire band, that is mean a good input and output matching. which reduce losses and increases output power.

The Kf test is used to determine the intended circuit stability, as illustrated in Figure 15, Kf is more than one over the whole design band.

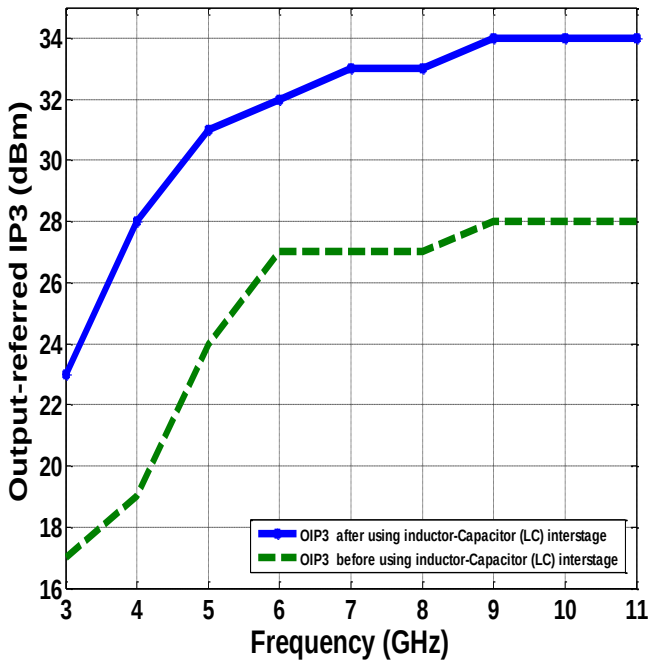

Figure 13 the Simulation of OIP3 with and without inductor-Capacitor (LC) inter-stage.

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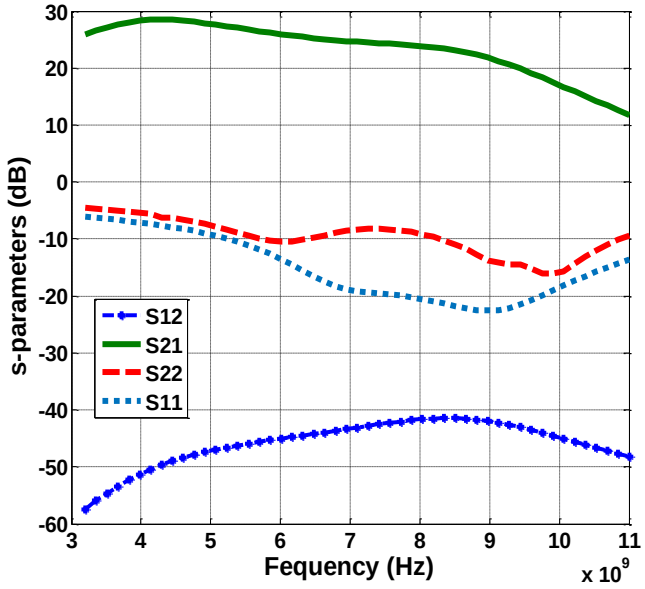

Figure 14 the Simulation of S-parameter.

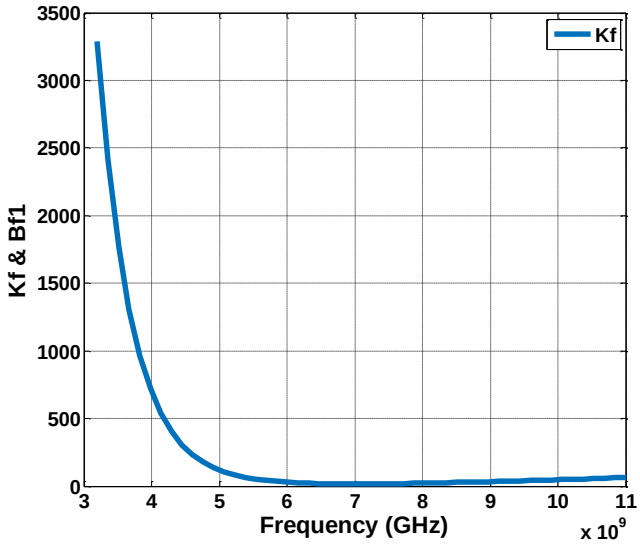

Figure 15 the Simulation of Kf and B1f.

Table 1 shows the performance comparison of the proposed circuit to the previously reported work, which illustrates that the circuit achieves a very good performance in the operating frequency band.

Table 1. Comparison between the proposed technique and the previous work .

Ref.	Tech. [nm]	Volt. [V]	Freq. GHz	Max. output dBm	S11(dB)	S22 (dB)	Dissipated Power (mW)	Max. PAE%
[10]**	HBT	3.4	1.7 to 2	28	N/A	N/A	N/A	40
[11]**	180	3.3	2.4	24.4	N/A	N/A	N/A	22
[12]**	45 nm	1.5	3.1-10.6	10	<-10	<-10	125	N/A
[13]*	65	1.2	3.1-10.6	6.8	<-7	<-10	15.5	29.5
[14]**	65	2.5	2.4	10.7	N/A	N/A	N/A	70
[15]*	180	1.8	2.5 to 5	14.6	<-1.29	<-10.11	77.3	47.5
[16]**	130	2	7.8 to 11.5	12	<-9	<-5	58	20
This work*	**130**	**1.8**	**3.1 to 10.6**	**26.4**	<-10	<-7	**34**	**54**

*Simulation results ** Measurements

VI. CONCLUSION

The design of a wideband hybrid class-F class-E PA with a proposed inductor-capacitor (LC) interstage is proposed. It is pointed out that the Class-F PA stage is the best driver for the class-E power amplifiers as it increases transmitter output power ,allows wideband RF transmission and improves the PAE of the proposed circuit. The proposed inductor-capacitor (LC) interstage improved the linearity of the proposed PA. The proposed circuit realizes a PAE above 54% with an output power greater than 26 dBm. Furthermore, the power gain is greater than 27 dB while the group delay variation is ±44 ps through the band from 3.1 to 10.6 GHz, which is a higher performance comparison to the previously reported work. The proposed power amplifier aimes to satisfy the requirements of 5G NR at 3.5GHz in terms of linearity, power-adding efficiency, and output power.

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