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A Power Efficient and Fast Locking CMOS Design of All-Digital Phase-Locked Loop

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ABSTRACT

The phase-locked loop (PLL) is the critical clock module in the System on Chip (SoC). PLL is a very complex process since it includes various parameters which are directly related to the performance of the PLL. Fast locking and low power consumption are the most important parameters in Digital PLL (DPLL). In this paper, a DPLL has been proposed and simulated to satisfy the requirements of RF applications. Digitally Controlled Oscillator (DCO) is the core of the DPLL which affects its overall performance, so an enhanced DCO structure has been proposed in a ring topology. The delay element of the ring oscillator is a Bulk Driven (BD) inverter which offers a promising enhancement in power consumption. The proposed DPLL scheme has been simulated using TSMC 65nm CMOS technology. Using 0.4V BD XNOR gate as a delay element of the ring oscillator, the output power is reduced to 61.74 µw, also the DPLL has produced 409MHz output frequency with a high speed of 23 ns locking time.

Keywords: *Analog Phase Locked Loop (APLL); Digital Phase Locked Loop (DPLL); Digitally Controlled Oscillator (DCO); Phase Frequency Detector (PFD); Bulk Driven (BD)*

1. INTRODUCTION

A Phase-locked loop (PLL) is an essential and major component in many communication systems. PLL is characterized as a circuit that enables a specific system to track another one. More precisely, PLL is a frequency synthesizer that is commonly used in analog, digital, RF, and embedded systems to generate a high-frequency clock from a low-frequency reference clock that often comes from a crystal oscillator. Nowadays most PLL architecture is introduced with digital circuits, where DPLL gain more interest than their analog counterparts for the significant benefits of digital systems. These benefits include progress in performance, reliability, speed, and reduction in cost and size. Also, DPLL alleviates many problems associated with Analog PLL (APLL), such as the sensitivity of the voltage-controlled oscillator to temperature and power supply variations, the sensitivity of analog multipliers (the most familiar error detectors used in APLL) to DC drifts, and Self-acquisition of APLLs is often slow and unreliable[1].

It is well-Known that DPLL consists of Phase Frequency Detector (PFD), Digital Loop Filter (DLF), Digitally controlled Oscillator (DCO), and Frequency Divider (FD), as shown in Fig. 1. The PFD compares the reference frequency with the oscillator output frequency and generates an error signal proportional to the difference between the two signals. This error signal is filtered by LPF and produces a control signal for the oscillator. The actual clock generated by a PLL comes from the controlled oscillator where the control signal tracking the oscillator frequency generating the desired one. The DCO is the cornerstone of DPLL as it provides the DPLL output clock signal. The most significant design consideration of DPLL is how it can be designed with low power, fast locking, and small area. DCO is the most power-hungry part of the DPLL which consumes over 50 percent of the power of the

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DPLL. Reduction of power consumption of the DCO is very important for low power DPLL design. Many techniques have been developed to design the DPLL in better performance. DPLL becomes more attractive as the efficiency and cost of digital very large-scale integration (VLSI) design technology improves. The frequency difference is accurately calculated and converted to the control word of the digital oscillator by using a time-to-digital converter (TDC) and applying this functionality, the all-digital PLL (ADPLL) lock-in time is faster than the preceding DPLL[2]. A modern scheme for a non-continuous operation for frequency divider, phase-frequency detector, and charge pump to design a power-efficient, low-phase noise, and small area PLL for electronics biomedical implants have been introduced in this paper [3]. Also, this paper proposes an ADPLL scheme by applying power enhanced digital loop filter instead of a traditional one for power-efficient design[4].

Although there are other parameters characterized by performance in PLL, we are focusing on the reduction of the power consumption and improving locking time. In VLSI systems power consumption includes dynamic power, static power, and leakage power. Dynamic power consumption arises from the switching between two separate voltages of load capacitance and is dependent on the operating frequency, as can be seen in eq. 1.

$$P_D = C_L V^2 F \qquad (1)$$

Where:
P_D is the dynamic power
C_L is the total capacitance seen at the output
V is the supply voltage
F is the operating frequency

Direct path short circuit currents between supply (VDD) and ground (VSS) contribute static power, which is dependent on leakage current. [5].

In this paper, a new design has been proposed to decrease the power consumption of the DPLL by the elimination of the direct path between the supply voltage and the ground by using the XNOR gate as an inverter and also reduces the supply voltage by applying a BD technique which reduces the threshold voltage of the transistor.

This paper is organized as follows. Section 2 presents the proposed architecture of DPLL. Results are presented in section 3. Finally, the key contributions of the paper are summarized in section 4.

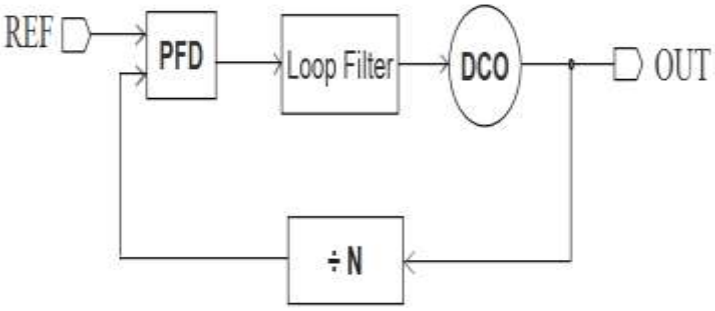


Fig. 1. Implementation of DPLL

2. PROPOSED ARCHITECTURE

In this section, we discuss the DPLL components and focus on our contribution to boosting the DCO performance.

- **Phase Frequency Detector**

The phase detector circuit compares the phase difference of its inputs and produces an output proportional to this phase difference. A usual example of a phase detector in APLL is the exclusive OR (XOR). The transition from the unlocked loop to the locked loop is an actual nonlinear phenomenon because the phase detector always senses unequal frequencies. The acquisition range is on the order of the loop filter frequency ω_{LPF}, where the loop locks only if the difference between ω_{in} and ω_{out} is less than relatively ω_{LPF}.

$$\omega_{in} - \omega_{out} < \omega_{LPF} \qquad (2)$$

The acquisition range reduces if ω_{LPF} is decreased in order to overcome the ripple on

the control voltage. Despite, if the input frequency has an exactly controlled value, it is necessary to provide a wide acquisition range because the center frequency of the VCO may vary substantially with process and temperature. In such case to repair the acquisition problem, the current PLL combines frequency detection in conjunction with phase detection[6].

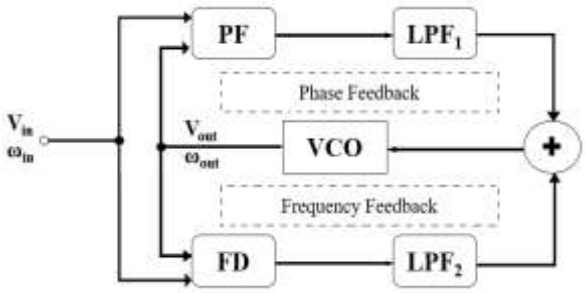


Fig. 2. Addition of frequency detection to increase the acquisition range

- **Digitally Controlled Oscillator**

Digital controlled oscillators (DCOs) are the heart of ADPLL circuits. Different DCO designs with various operating frequency ranges have been documented, one is the path delay oscillator that uses logic gates to construct a ring structure, the Schmitt trigger current-driven oscillator with a large number of MOS transistors is the second type of DCO, and another type consumes large size and a large amount of hardware, based on current starved ring oscillators[7]. The delay element is a critical component of an oscillator architecture,and the overall performan ce of a DCO device is directly influenced by its tuning. There are two parameters that modulate a ring oscillator's output frequency. The first is each delay stage's propagation delay time and the other is the total number of closed-loop delay cells.

DCO power consumption is a very important issue to improve the overall power consumption of DPLL, so we used a new technique in designing the delay element to reduce the power consumption of the DCO. Firstly, to reduce the static power by eliminating the direct path between supply voltage and ground, so XNOR gate functioning as an inverter has been used as the delay cell. One XNOR gate input terminal is grounded, and the signal is applied to the other terminal in order for the circuit to act as an inverter as shown in Fig. 3.

DCO designs with the proposed XNOR displays substantial power saving due to the reduction in the leakage current. In the switch network, binary weighted MOS transistors have been used and binary bits added to these transistors to control the delay of each stage. Different transistors operate with unequal widths and the resistance of the transistor network various with changing bit patterns, which further modulates the circuit delay, therefor different frequency components are generated as controlled using a digital input word[7].

While the static power and dynamic power are directly proportional to the supply voltage and the square of supply voltage, respectively. Accordingly, if we want to decrease the power losses, we should decrease the supply voltage. On the other hand, there are some issues relating to decreasing the supply voltage, such as reduced drivability of the MOS Transistor, reduced signal swings, increased threshold variations, and threshold voltage limitation. In scaled-down systems, lowering the threshold voltage causes issues such as rising parasitic effects, short channel effects, and leakage current. There are some techniques used to reduce supply voltages, one of them is the Bulk Driven technique.

When the bulk voltage of a MOS transistor is connected to a voltage source, the S and D junctions remain reverse-biased, so the system continues to work normally, but some of its characteristics may change. For NMOS

transistor assume the drain and source voltages are grounded $V_D = V_S = 0$, and the gate voltage is less than the threshold voltage $V_G < V_{TH}$, therefore, under the gate a depletion region is created but there is no inversion layer. If the bulk voltage V_B being more negative, more holes are attracted to the substrate, leaving a larger negative charge behind, As a result, the depletion area increases[8].

Equation of threshold voltage becomes

$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{2\varphi_F + v_{SB}} - \sqrt{|2\varphi_F|}\right) \quad (3)$$

Table 1 highlighting parameters definition.

V_{TH0}	The threshold voltage at zero bulk source voltage
φ_F	The Fermi potential
γ	The body effect coefficient
V_{SB}	The source bulk voltage difference

Table 1 Parameter Definition

So, the bulk-driven transistor is works like a depletion-type device.

The threshold voltage can be electrically eliminated without any technology modification. This will impact the depletion region thickness associated with the inversion layer When the gate to source voltage is fixed to sufficiently establish conducting channel and apply voltage to the bulk. Because of this method, the operating time of the MOS transistor is decreased, the threshold voltage of the MOS transistor is decreased and the output is achieved at a low supply voltage. This design is illustrated in Fig. 4.

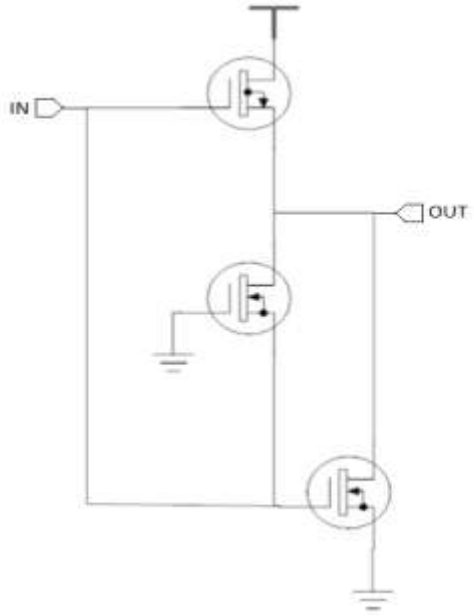


Fig. 3. XNOR gate as an inverter

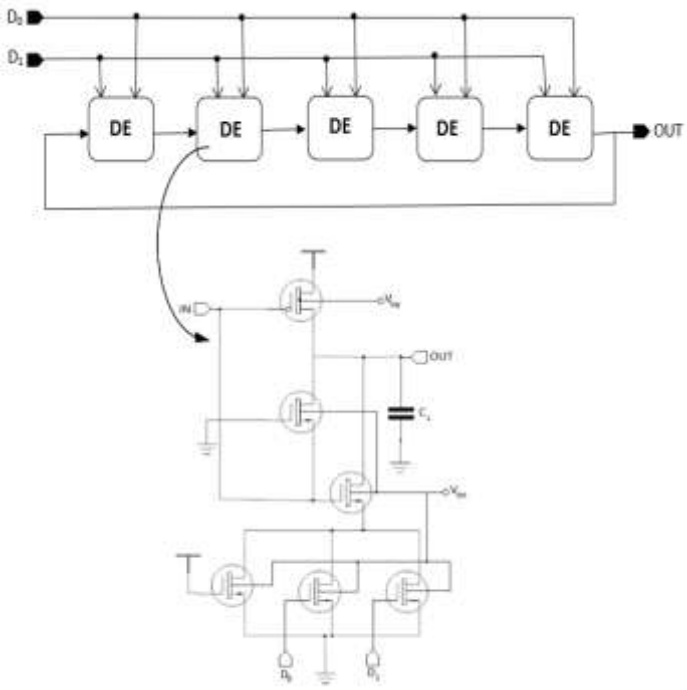


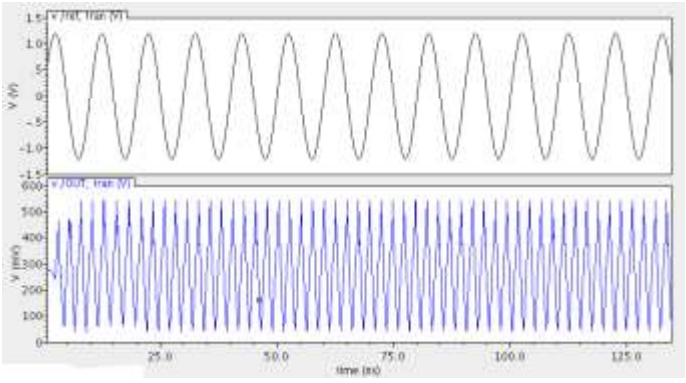
Fig. 4. Schematic of Digitally controlled Ring Oscillator circuit

I. SIMULATION RESULTS

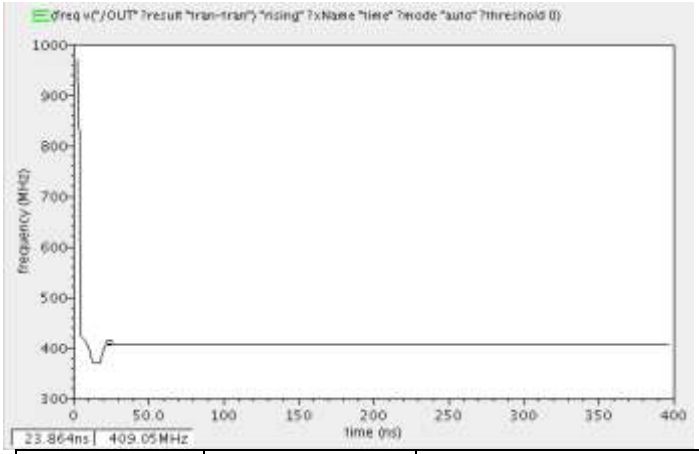
Table 1 shows a comparison among three configurations of DCO, using the conventional inverter, XNOR based inverter, and XNOR with BD technique inverter as a Delay Element (DE) of

the DCO. The complete block diagram of the DPLL is implemented in a 65 nm CMOS process. The PLL using XNOR with BD technique inverter as a Delay Unit operates across a supply voltage of 0.6 V and achieves an operating frequency of 409 MHz while consuming a static power of 61.74 µW and dynamic Power of 0.074 µW. The PLL output is shown in Fig. 5.

Referring back to the research aims, the power consumption of the system improved to a satisfactory value, which makes this design applicable for many analog and digital systems. Also, the period jitter of the proposed architecture is 28.96 ns.



(a)



(b)

Fig. 5. (a) DPLL output signal, (b) DPLL output Frequency

II. Conclusions

DPLL structure using enhanced DCO achieves excellent power efficiency and fast locking operation is presented in this paper. The DCO based ring topology with XNOR delay element reduces the leakage current and the Bulk Driven technique reduces the operating supply voltage so total power dissipation is extremely decreased. This DPLL architecture is well suited for use in very low power and high-speed applications as a result of this achievement.

This DPLL is designed and implemented using 65nm CMOS technology for a frequency of 409 MHz at supply voltage 0.6V. Operating with 0.4V bulk voltage the power dissipation reduced to 61.74 µW, and the locking time recorded 23ns. The proposed work will be a strong guide for future advanced DPLL. In table 3, the proposed DPLL's performance is compared to that of a state-of-the-art PLL. From this comparison, it is clear that the power consumption of our proposed method has been enhanced to a sufficient value.

	Conventional Inverter	**XNOR based inverter**				**XNOR with BD technique inverter**			
		D0 = 0 D1 = 0	D0 = 1 D1 = 0	D0 = 0 D1 = 1	D0 = 1 D1 = 1	D0 = 0 D1 = 0	D0 = 1 D1 = 0	D0 = 0 D1 = 1	D0 = 1 D1 = 1
V (v)	1	1				0.6			

CL (pF)	0.01	0.01				0.01			
Output Frequency	11.37 GHz	1.557 GHz	1.726 GHz	1.767 GHz	1.78 GHz	574 MHz	658 MHz	668 MHz	672.7 MHz
Delay (ns)	0.4116	2.016	2.198	2.089	2.04	9.96	11.02	10.56	10.21
Static Power (µw)	13890	203.2	214.3	216.7	217.8	11.43	11.68	11.7	11.7
Dynamic Power (µw)	113.7	15.57	17.26	17.67	17.8	2.06	2.36	2.4	2.42

Table 2 comparison of using the conventional inverter, XNOR based inverter and XNOR with BD technique inverter as a delay element of the DCO.

	This work	**EDSSC 2016 [9]**	**2010 [10]**	**CICN 2016 [11]**	**ISSCC 2018 [12]**	**ISSCC 2016 [13]**	**CICC 2020 [14]**	**ISSCC 2019 [15]**
Technology (nm)	**65**	180	130	90	65	65	22	10
Supply Voltage (v)	**0.6**	1.8	1.2	1	n.a.	1.2	0.5-0.9	0.9
Ref. Freq.(MHz)	**100**	n.a.	250	100	52	40	20-200	19.2-100
Output Freq.(MHz)	**409**	800	1.75×10^3	800	$(3.7\text{-}4.1)\times10^3$	2.4	3.2×10^3 @ 0.8v	3.2×10^3
Power(µw)	**61.74**	18.2×10^3	75×10^3	123.89	5.28×10^3	360	213	430
Lock time (ns)	**23**	7.52×10^3	80	2.82	5.6×10^3	n.a.	200	n.a.

Table 3 Performance comparison of proposed architecture with state-of-the-art designs

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ملخص

الطور المغلق هو وحدة الوقت المهمة فى النظام على الرقاقة. الطور المغلق هو عملية معقدة جدا حيث يحتوى على العديد من المعاملات التى تتناسب مباشرة مع اداء هذا الطور. سرعة حلقة القفل و الاستهلاك المنخفض للطاقة من أكثر المعاملات اهمية فى دوائر الطور المغلق كليا، هذا التصميم من الطور المغلق تم تصميمه و محاكاته فى هذا البحث حتى يتناسب مع متطلبات تطبيقات تردد الراديو.

المذبذب الرقمى هو نواة الطور المغلق والذى يؤثر على الاداء الكلى لهذا الطور، لذلك المذبذب الرقمى المحسن يتم عرضه فى بنية حلقية. عنصر التأخير فى المذبذب الرقمى هو العاكس باستخدام تقنية Bulk Driven (BD) والذى يقدم تعزيز واعد فى تقليل استهلاك الطاقة.

مخطط الطور المغلق المقترح تمت محاكاته باستخدام برنامج TSMC و تكنولوجيا 65 نانومتر لشبه موصل أكسيد الفلز المكمل. استخدمة تقنية Bulk Driven على البوابة المنطقية XNOR كعنصر تأخير فى المذبذب الرقمى، خفضت انتاج الطاقة الى 61.74 µw، أيضا تردد الخرج للطور المغلق كليا قيمته 409 MHz مع زيادة سرعة وقت القفل الى 23 ns.